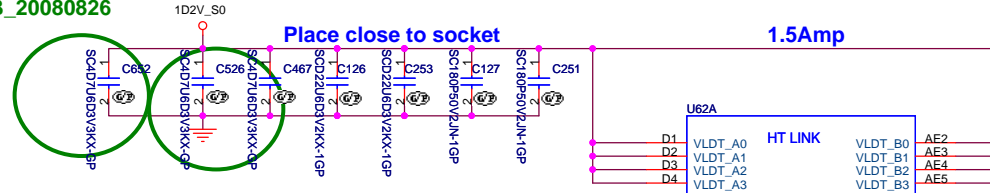


SB_20080826



2008/07/23

| State | Specification | Notes | 2M200100M2303 |
|----------|-----------------|-------|---------------|
| S0.C0.Px | Tcase Max | 3 | TBD |
| | NB COF | 1 | 400 MHz |
| | VID_VDDNB Min | 2 | 0.950 V |
| | VID_VDDNB Max | 2 | 0.950 V |
| | Startup P-state | | S0.C0.P7 |
| S0.C0.P0 | CPU COF | 1 | 2000 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 0.950 V |
| | IDD Max | 3 | TBD |
| S0.C0.P1 | CPU COF | 1 | 1800 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P2 | CPU COF | 1 | 1500 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P3 | CPU COF | 1 | 1300 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P4 | CPU COF | 1 | 1000 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P5 | CPU COF | 1 | 800 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P6 | CPU COF | 1 | 500 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| S0.C0.P7 | CPU COF | 1 | 300 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |

HT_NB_CPU_CAD_H0
HT_NB_CPU_CAD_L0
HT_NB_CPU_CAD_H1
HT_NB_CPU_CAD_L1
HT_NB_CPU_CAD_H2
HT_NB_CPU_CAD_L2
HT_NB_CPU_CAD_H3
HT_NB_CPU_CAD_L3
HT_NB_CPU_CAD_H4
HT_NB_CPU_CAD_L4
HT_NB_CPU_CAD_H5
HT_NB_CPU_CAD_L5
HT_NB_CPU_CAD_H6
HT_NB_CPU_CAD_L6
HT_NB_CPU_CAD_H7
HT_NB_CPU_CAD_L7
HT_NB_CPU_CAD_H8
HT_NB_CPU_CAD_L8
HT_NB_CPU_CAD_H9
HT_NB_CPU_CAD_L9
HT_NB_CPU_CAD_H10
HT_NB_CPU_CAD_L10
HT_NB_CPU_CAD_H11
HT_NB_CPU_CAD_L11
HT_NB_CPU_CAD_H12
HT_NB_CPU_CAD_L12
HT_NB_CPU_CAD_H13
HT_NB_CPU_CAD_L13
HT_NB_CPU_CAD_H14
HT_NB_CPU_CAD_L14
HT_NB_CPU_CAD_H15
HT_NB_CPU_CAD_L15

HT_NB_CPU_CLK_H0
HT_NB_CPU_CLK_L0
HT_NB_CPU_CLK_H1
HT_NB_CPU_CLK_L1

HT_NB_CPU_CTL_H0
HT_NB_CPU_CTL_L0
HT_NB_CPU_CTL_H1
HT_NB_CPU_CTL_L1

L0_CADIN_H0
L0_CADIN_L0
L0_CADIN_H1
L0_CADIN_L1
L0_CADIN_H2
L0_CADIN_L2
L0_CADIN_H3
L0_CADIN_L3
L0_CADIN_H4
L0_CADIN_L4
L0_CADIN_H5
L0_CADIN_L5
L0_CADIN_H6
L0_CADIN_L6
L0_CADIN_H7
L0_CADIN_L7
L0_CADIN_H8
L0_CADIN_L8
L0_CADIN_H9
L0_CADIN_L9
L0_CADIN_H10
L0_CADIN_L10
L0_CADIN_H11
L0_CADIN_L11
L0_CADIN_H12
L0_CADIN_L12
L0_CADIN_H13
L0_CADIN_L13
L0_CADIN_H14
L0_CADIN_L14
L0_CADIN_H15
L0_CADIN_L15

L0_CLKIN_H0
L0_CLKIN_L0
L0_CLKIN_H1
L0_CLKIN_L1

L0_CTLIN_H0
L0_CTLIN_L0
L0_CTLIN_H1
L0_CTLIN_L1

L0_CADOUT_H0
L0_CADOUT_L0
L0_CADOUT_H1
L0_CADOUT_L1
L0_CADOUT_H2
L0_CADOUT_L2
L0_CADOUT_H3
L0_CADOUT_L3
L0_CADOUT_H4
L0_CADOUT_L4
L0_CADOUT_H5
L0_CADOUT_L5
L0_CADOUT_H6
L0_CADOUT_L6
L0_CADOUT_H7
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L0_CADOUT_H13
L0_CADOUT_L13
L0_CADOUT_H14
L0_CADOUT_L14
L0_CADOUT_H15
L0_CADOUT_L15

L0_CLKOUT_H0
L0_CLKOUT_L0
L0_CLKOUT_H1
L0_CLKOUT_L1

L0_CTLOUT_H0
L0_CTLOUT_L0
L0_CTLOUT_H1
L0_CTLOUT_L1

SKT-CPU638P-GP-U2

62.10055.111

2ND = 62.10055.251

SKT-BGA638H176

HT_CPU_NB_CAD_H0
HT_CPU_NB_CAD_L0
HT_CPU_NB_CAD_H1
HT_CPU_NB_CAD_L1
HT_CPU_NB_CAD_H2
HT_CPU_NB_CAD_L2
HT_CPU_NB_CAD_H3
HT_CPU_NB_CAD_L3
HT_CPU_NB_CAD_H4
HT_CPU_NB_CAD_L4
HT_CPU_NB_CAD_H5
HT_CPU_NB_CAD_L5
HT_CPU_NB_CAD_H6
HT_CPU_NB_CAD_L6
HT_CPU_NB_CAD_H7
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HT_CPU_NB_CAD_H8
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HT_CPU_NB_CAD_H12
HT_CPU_NB_CAD_L12
HT_CPU_NB_CAD_H13
HT_CPU_NB_CAD_L13
HT_CPU_NB_CAD_H14
HT_CPU_NB_CAD_L14
HT_CPU_NB_CAD_H15
HT_CPU_NB_CAD_L15

HT_CPU_NB_CLK_H0
HT_CPU_NB_CLK_L0
HT_CPU_NB_CLK_H1
HT_CPU_NB_CLK_L1

HT_CPU_NB_CTL_H0
HT_CPU_NB_CTL_L0
HT_CPU_NB_CTL_H1
HT_CPU_NB_CTL_L1

SB

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_HT_LINK I/F (1/4)

Size

Document Number

A3

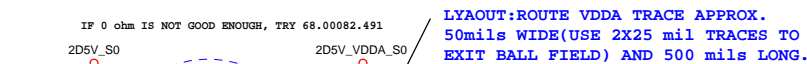
F7-GT

Date: Friday, August 29, 2008

Sheet 3 of 47

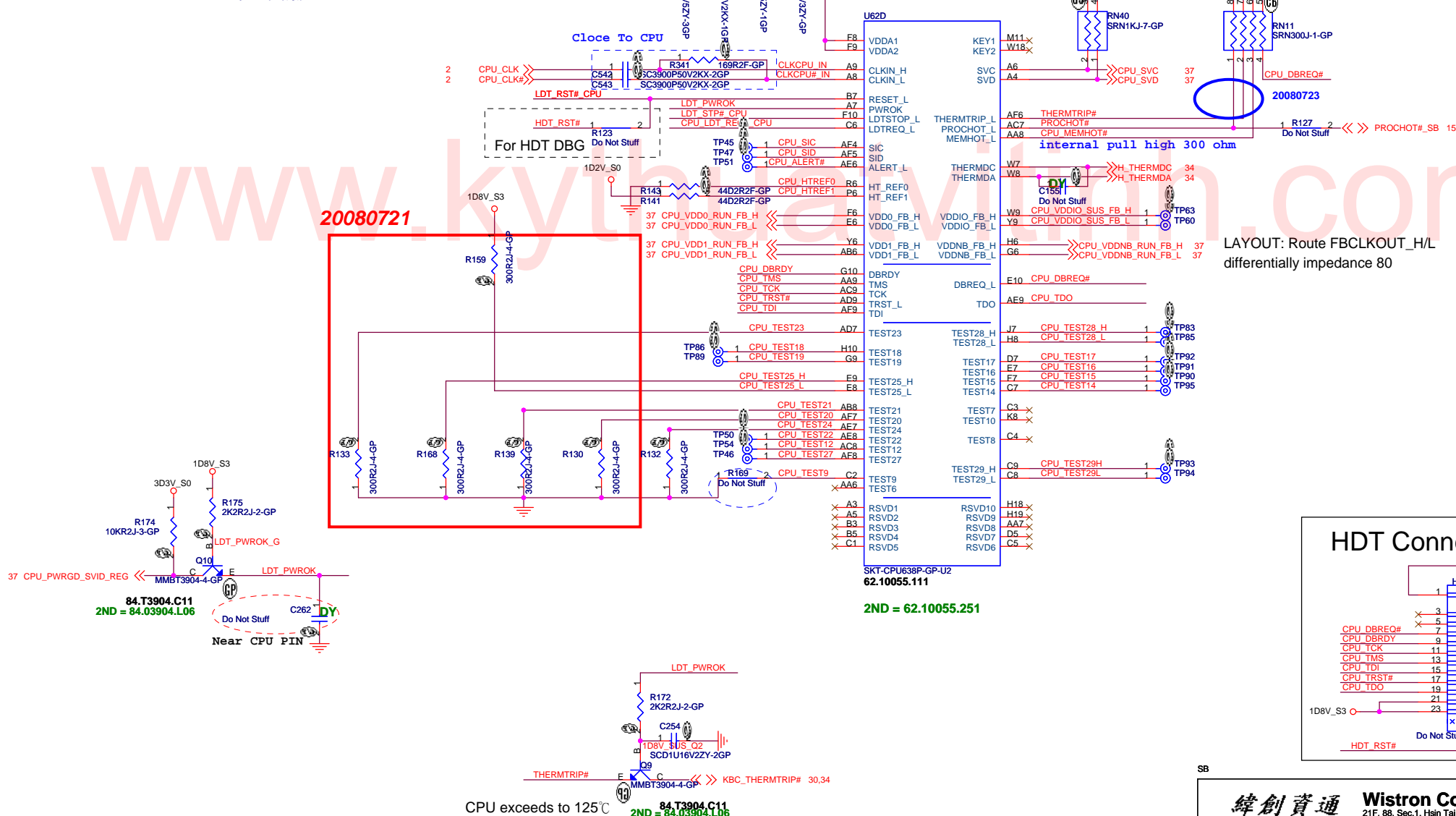
Rev

SB



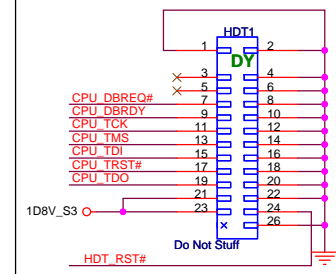
LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN



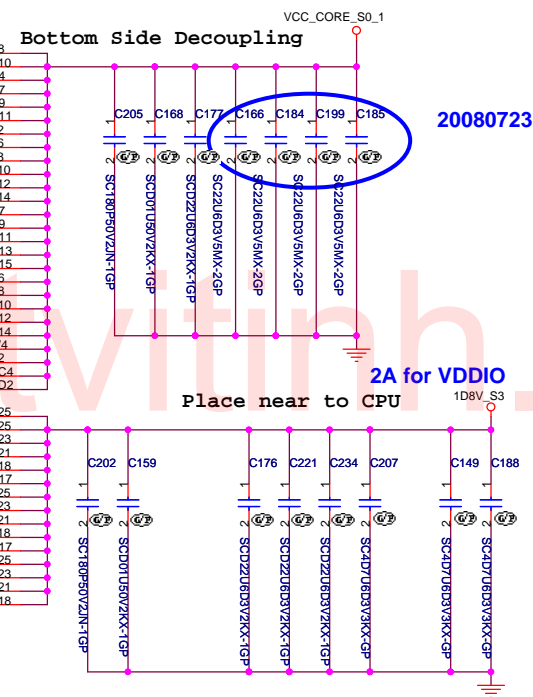
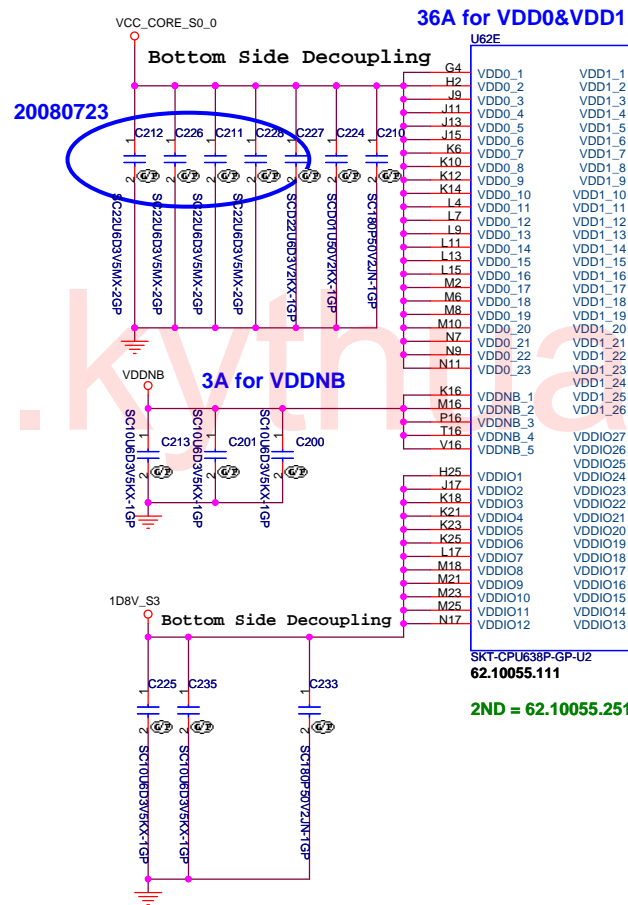
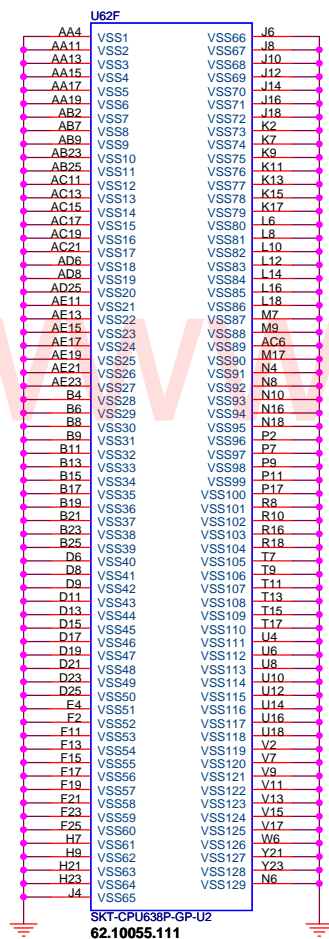
LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

HDT Connectors



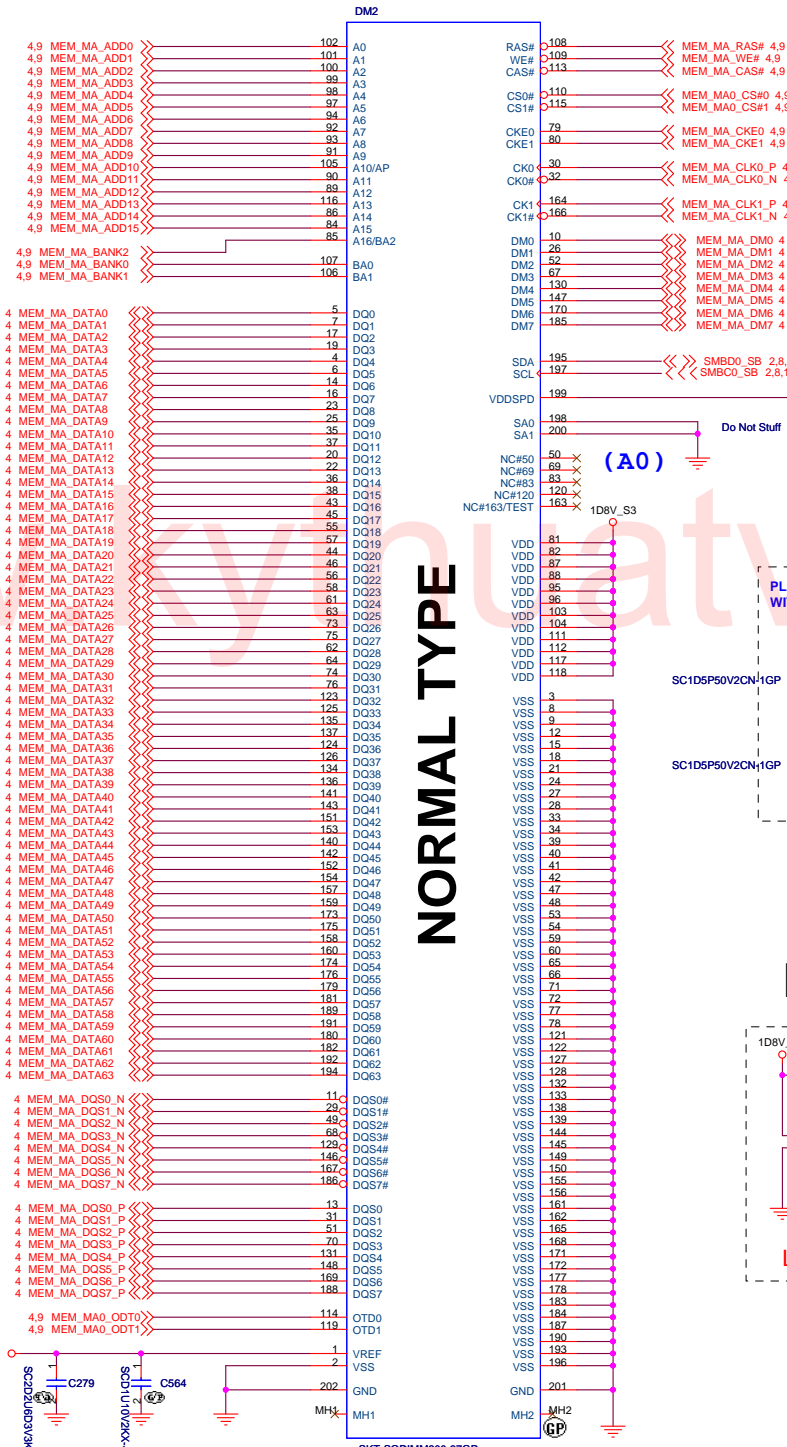
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|------------------------------------|-------------------------|-----------|---------|
| Title | | | |
| CPU_Control&Debug_(3/4) | | | |
| Size | Document Number | Rev | |
| A3 | F7-GT | SB | |
| Date: | Friday, August 29, 2008 | Sheet | 5 of 47 |

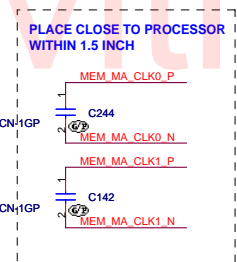
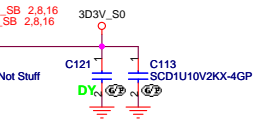


SB

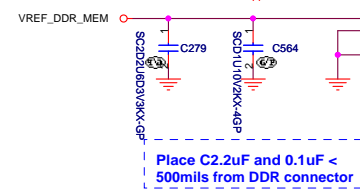
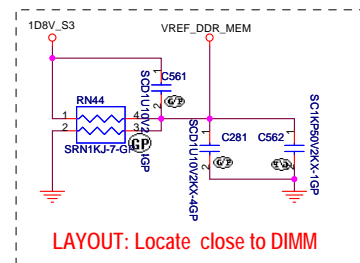
| | |
|--|---------------------------------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title CPU_Power_(4/4) | |
| Size A3 | Document Number F7-GT |
| Date: Wednesday, August 20, 2008 | Sheet 6 of 47 |
| Rev SB | |



NORMAL TYPE

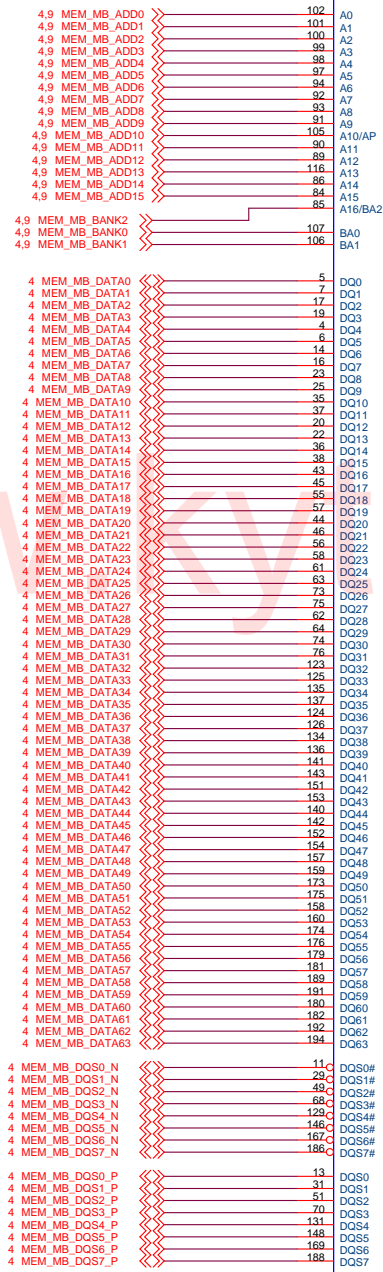


DDR_VREF

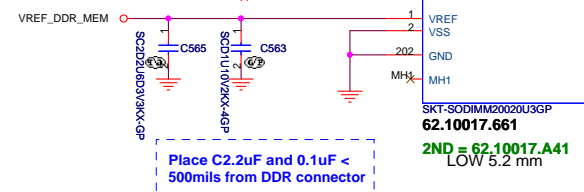
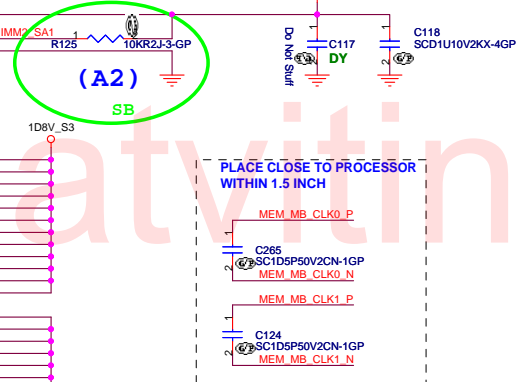
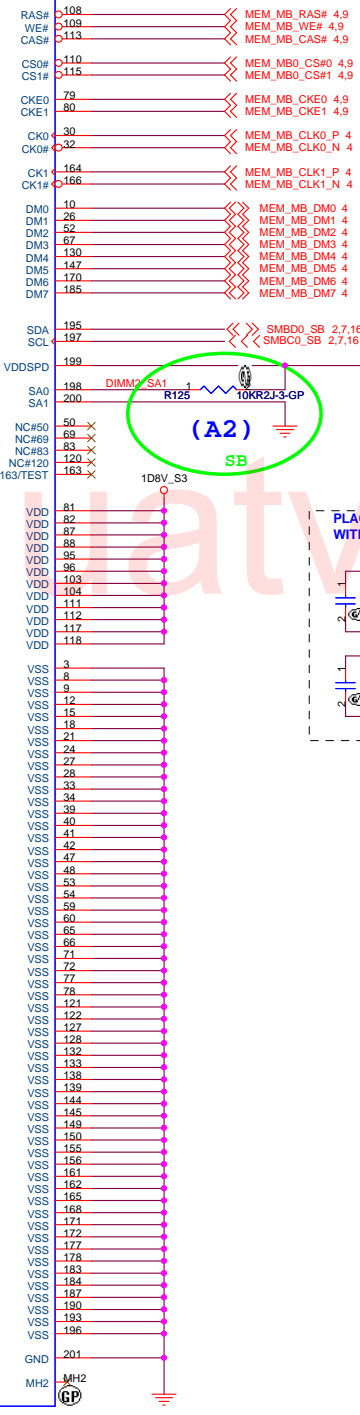


Place C2.2uF and 0.1uF < 500mils from DDR connector

HI 9.2mm
62.10017.E21
2ND = 62.10017.A51

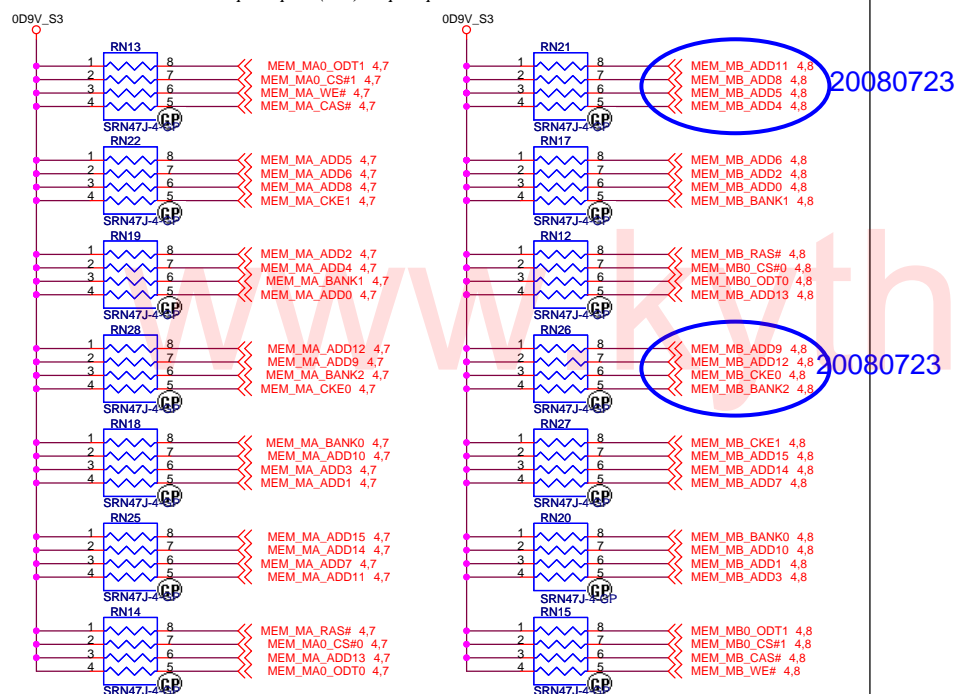


REVERSE TYPE



PARALLEL TERMINATION

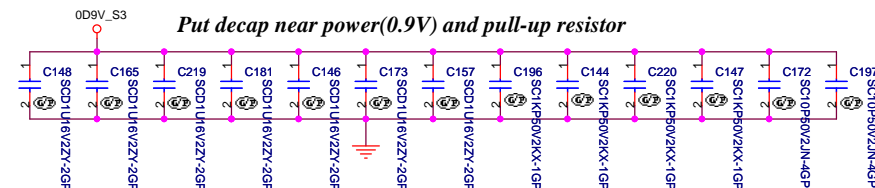
Put decap near power(0.9V) and pull-up resistor



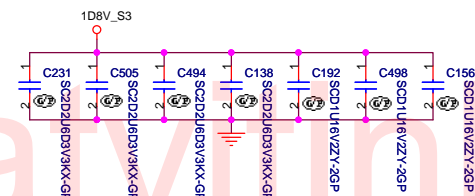
Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

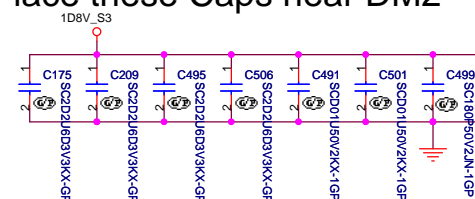


Place these Caps near DM1



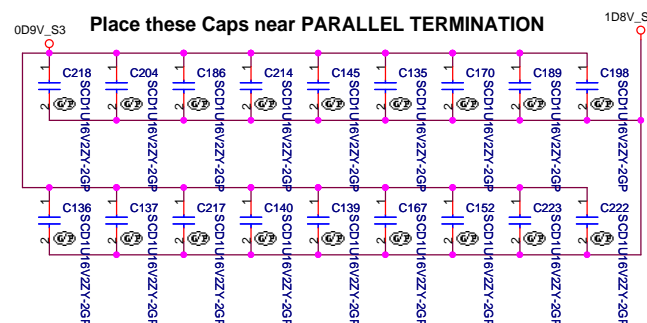
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to 0D9V S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to 0D9V S3

Place these Caps near PARALLEL TERMINATION



SB

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Taipei Hsien 221, Taiwan, R.O.C.

| | |
|-------|--|
| Title | |
|-------|--|

DDR DAMPING & TERMINATION

| Size | Document Number | Rev |
|------|-----------------|-----|
|------|-----------------|-----|

| | | |
|----|--------------|----|
| A3 | F7-GT | SB |
|----|--------------|----|

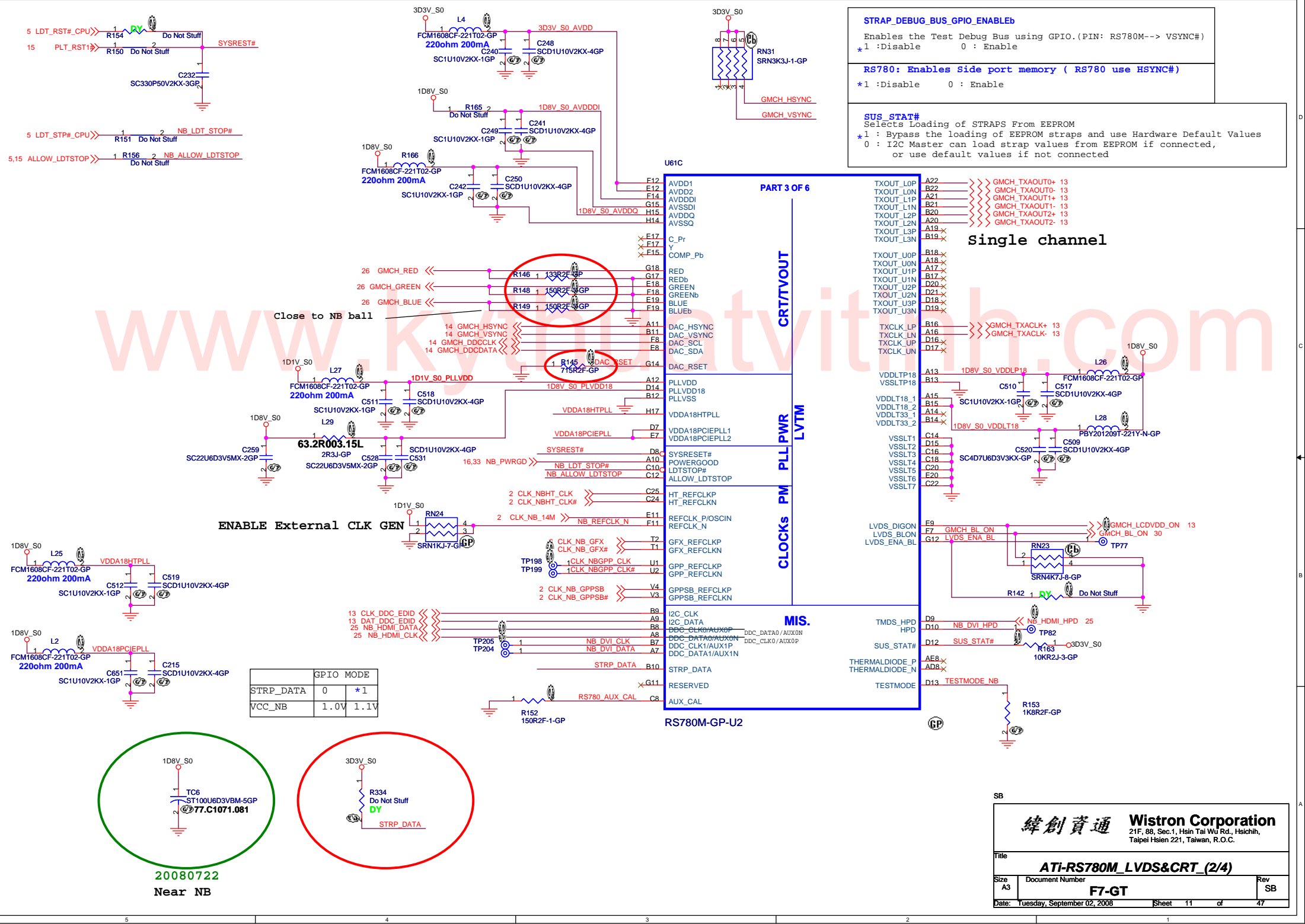
Date: Friday, August 29, 2008 Sheet 9 of 47

| | |
|--|---|
| | 1 |
|--|---|



1

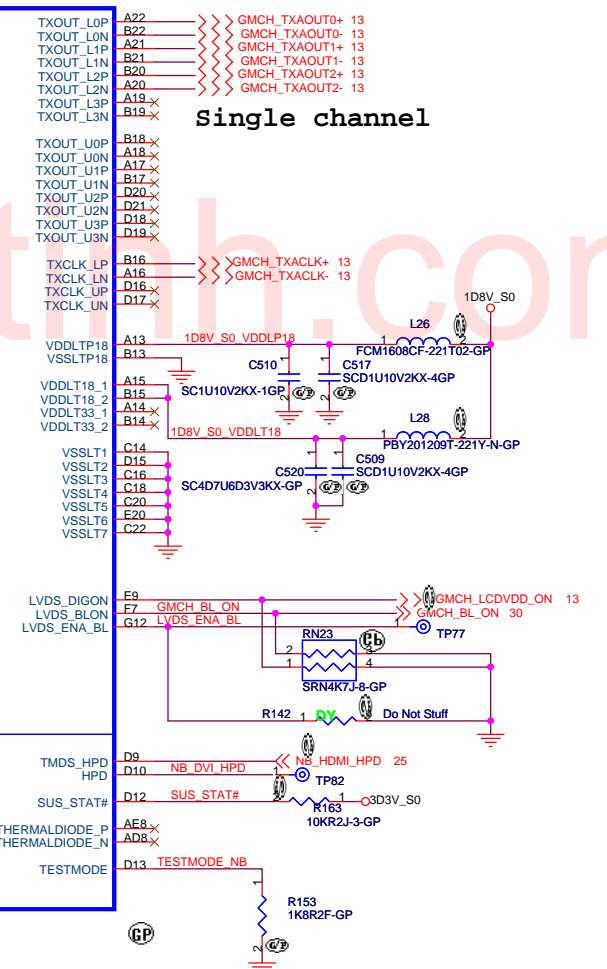




STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

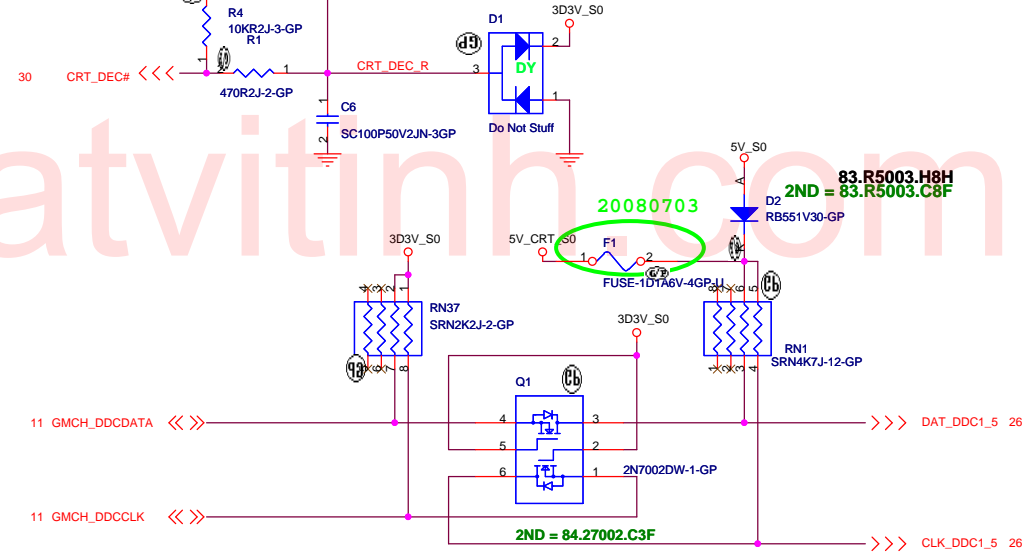
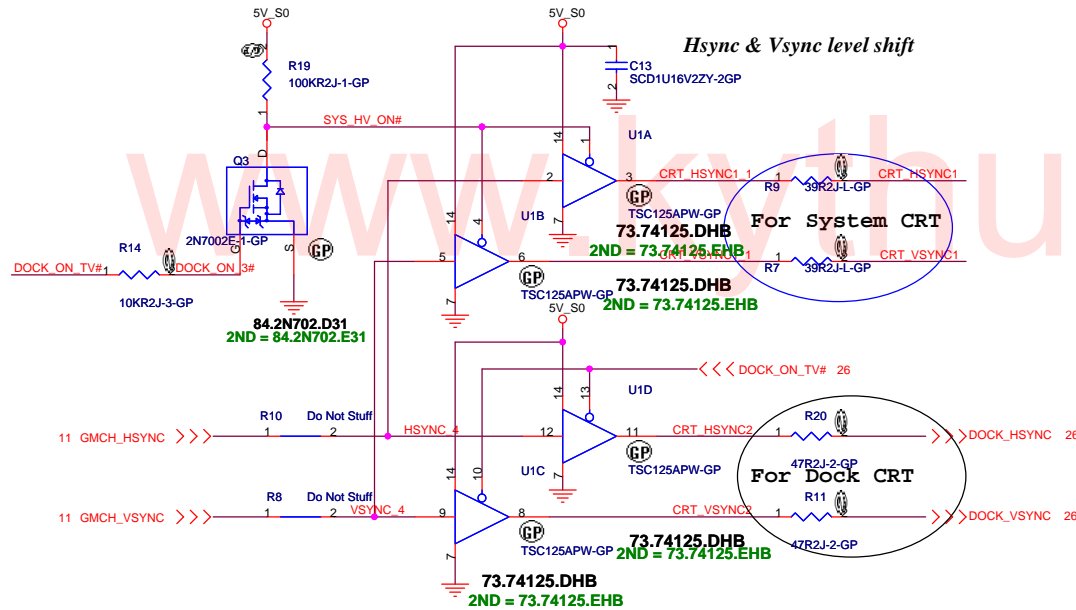
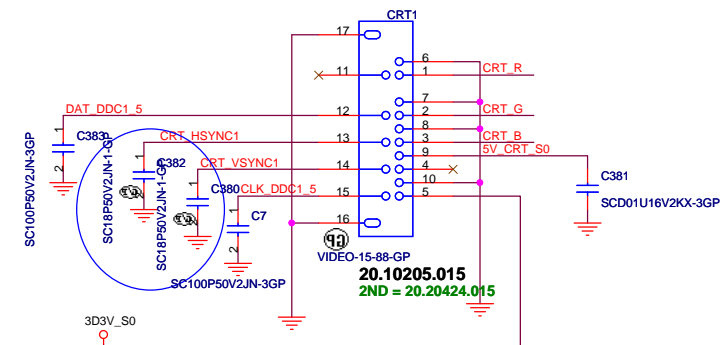
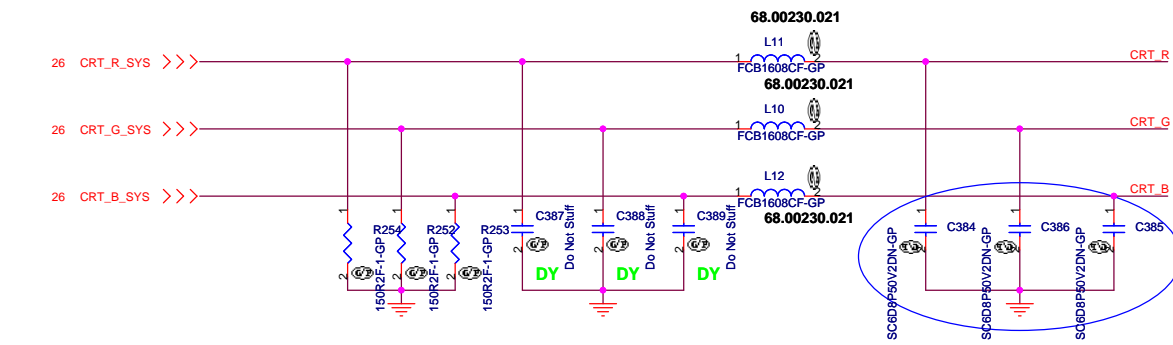


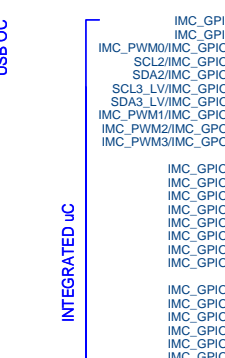
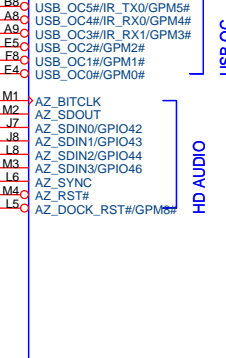
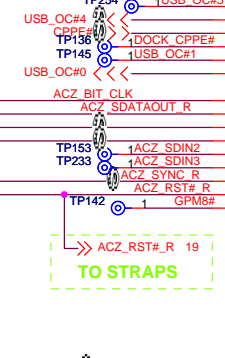
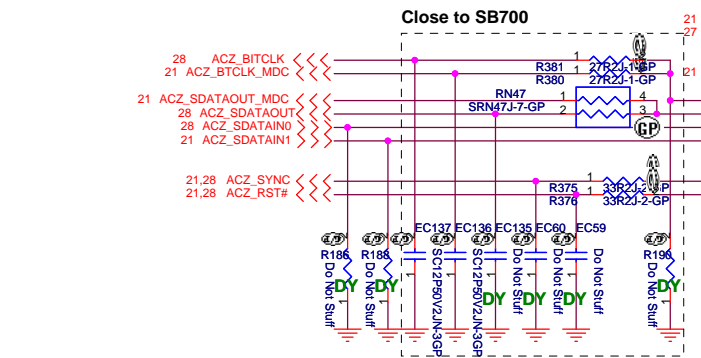
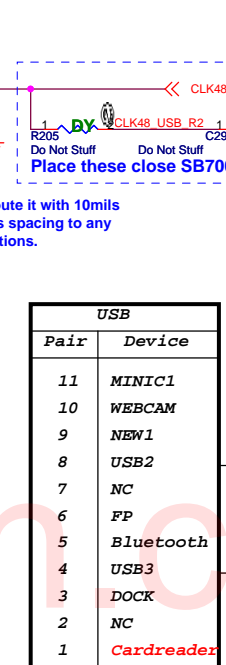
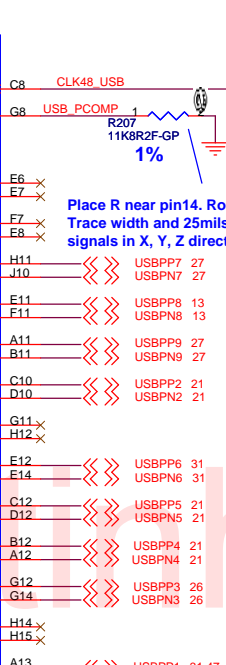
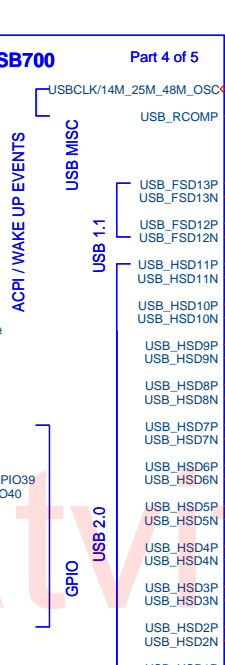
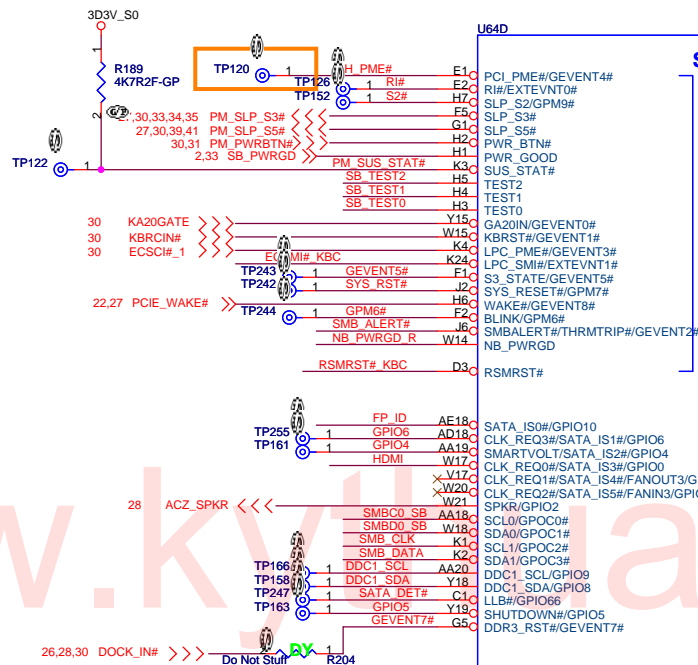
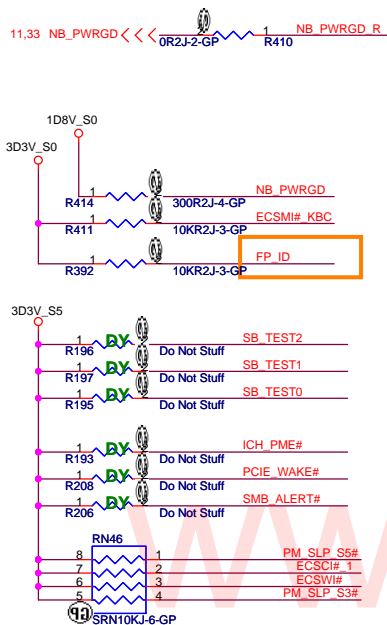
緯創資通 Wistron Corporation
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Title
ATI-RS780M_LVDS&CRT_(2/4)

Size A3 Document Number **F7-GT** Rev SB

Date: Tuesday, September 02, 2008 Sheet 11 of 47





PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

SATA HDD

SATA ODD



U64B

SB700
Part 2 of 5



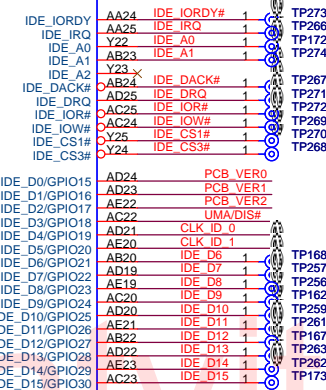
SERIAL ATA

ATA 66/100/133

SATA PWR

HW MONITOR

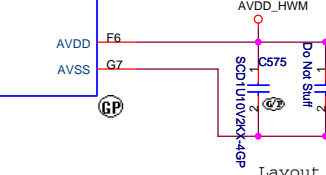
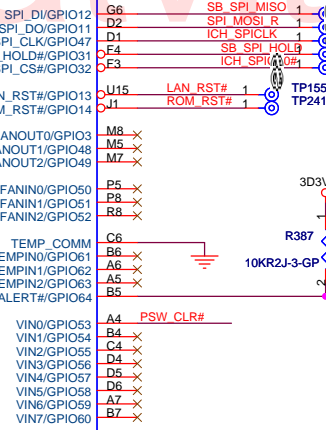
SB700-1-GP-U1
71.SB700.M02



SPI ROM

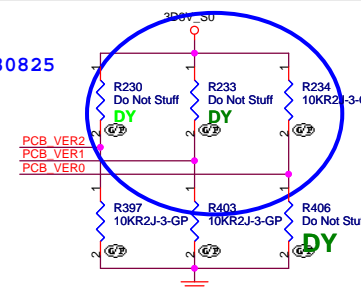
SATA PWR

HW MONITOR

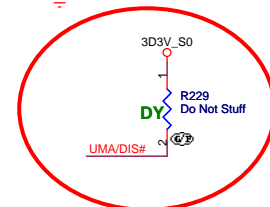


Layout connect to Cap then GND

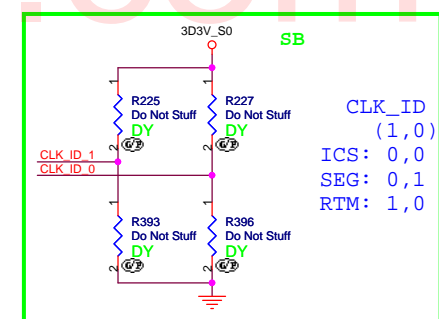
20080825



PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 0,1,1



20080722

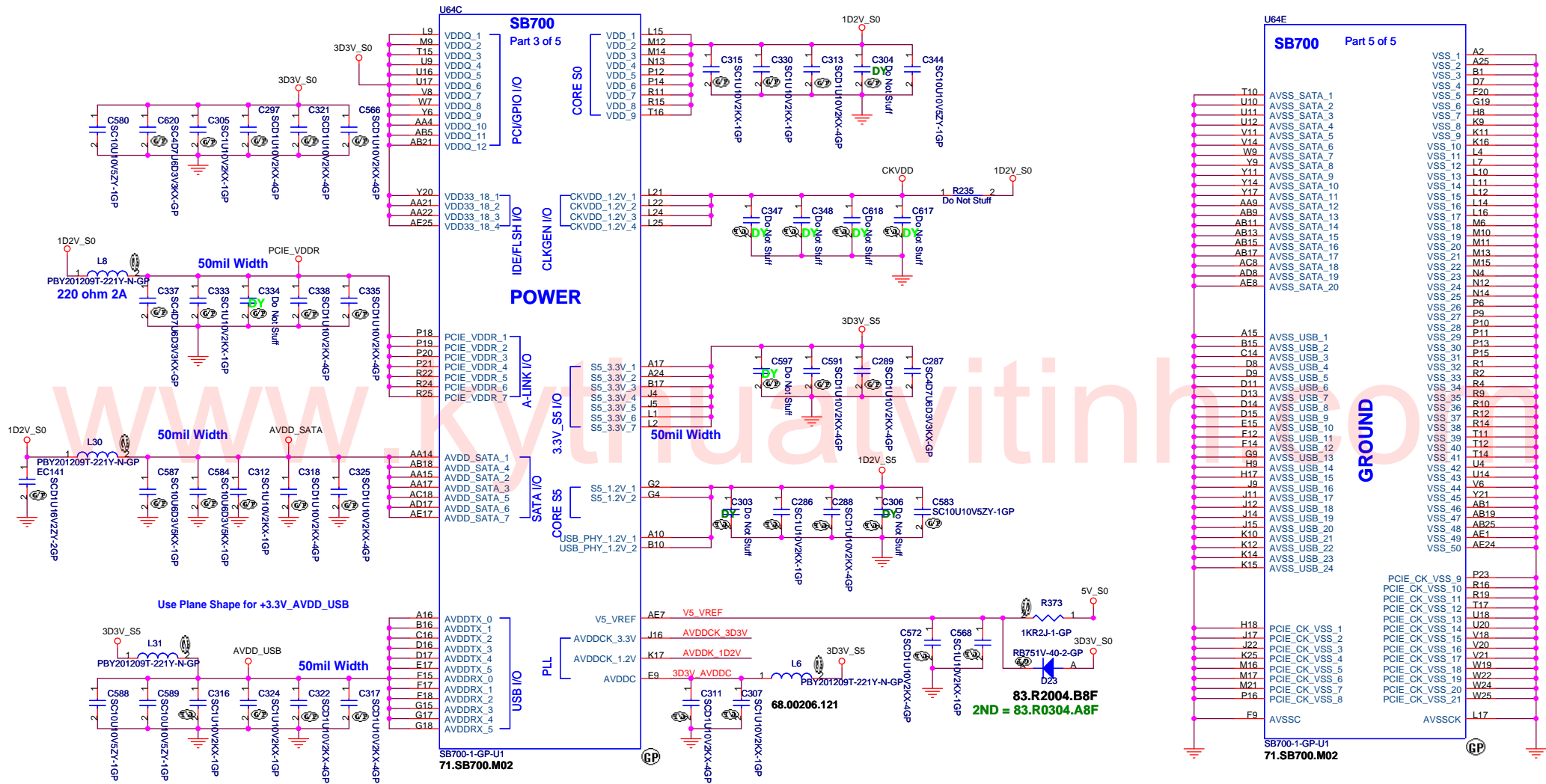


CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

SB

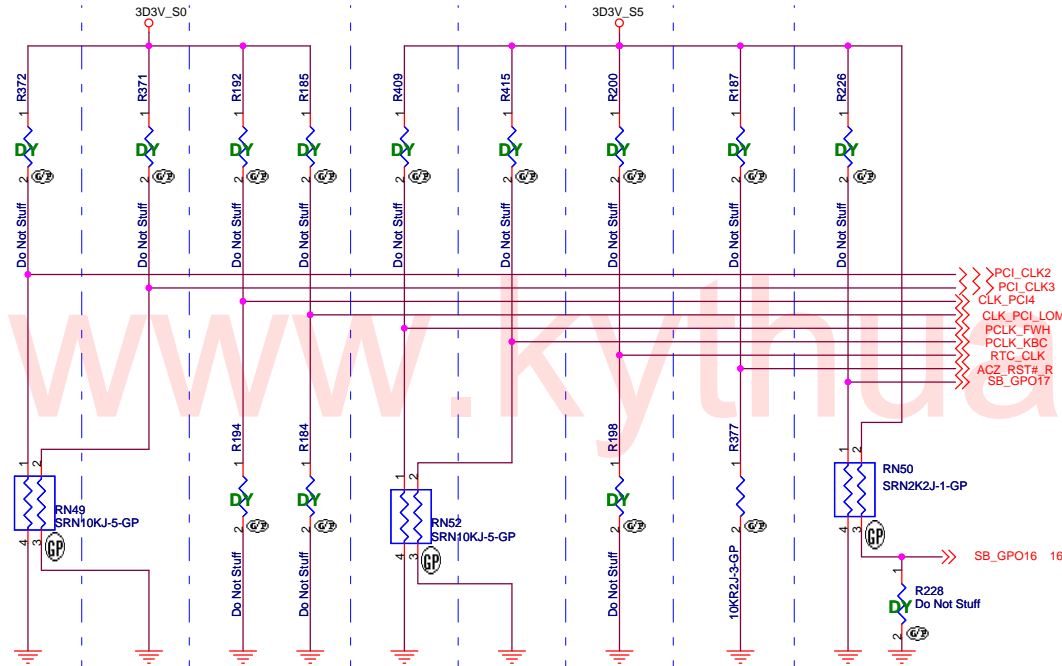
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Taipai Hsien 221, Taiwan, R.O.C.

| | | | | |
|--------------------------|-------------------------|-------|-------|-----|
| Title | | | | |
| ATI-SB700 SATA-IDE (3/5) | | | | |
| Size | Document Number | | | Rev |
| A3 | F7-GT | | | S |
| Date: | Friday, August 29, 2008 | Sheet | 17 of | 47 |

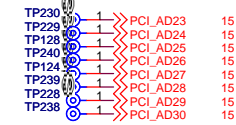


REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS



| | PCI_CLK2 | PCI_CLK3 | CLK_PCI_LOM CLK_PCI4 | PCLK_FWH | PCLK_KBC | RTCCLK | AZ_RST# | SB_GPO17, SB_GPO16 |
|-----------|---|--------------------------------------|-------------------------|----------------------------|---|---|------------------------------------|--|
| PULL HIGH | WatchDOG (NB_PWRGD) ENABLED | USE DEBUG STRAPS | RESERVED | IMC ENABLED | CLKGEN ENABLED (Use Internal) | INTERNAL RTC DEFAULT | ENABLE PCI ROM BOOT | ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT |
| PULL LOW | WatchDog (NB_PWRGD) DISABLED DEFAULT | IGNORE DEBUG STRAPS DEFAULT | | IMC DISABLED DEFAULT | CLKGEN DISABLED (Use External) DEFAULT | EXT. RTC (PD on X1, apply 32KHz to RTC_CLK) | DISABLE PCI ROM BOOT DEFAULT | L, H = LPC ROM L, L = FWH ROM |

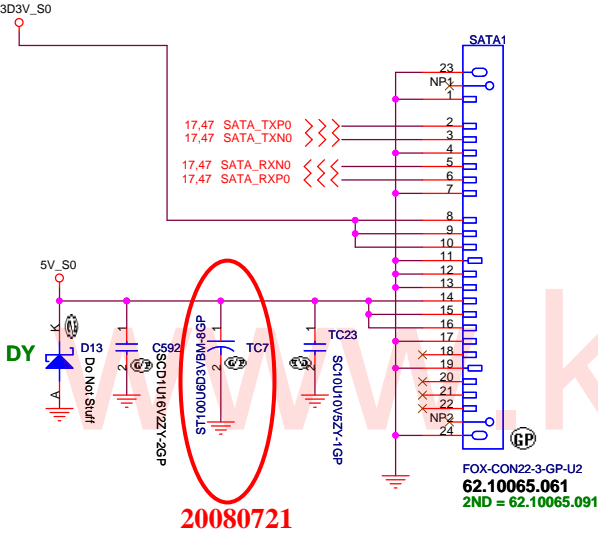
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

| | PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 | PCI_AD30 PCI_AD29 |
|-----------|-----------------------------------|-----------------------------|-------------------------------|-----------------------------|---|-----------------------|----------------------|
| PULL HIGH | USE LONG RESET (DEFAULT) | USE PCI PLL (DEFAULT) | USE ACPI BCLK (DEFAULT) | USE IDE PLL (DEFAULT) | USE DEFAULT PCIE STRAPS (DEFAULT) | Reserved (DEFAULT) | Reserved |
| PULL LOW | USE SHORT RESET | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | Reserved | |

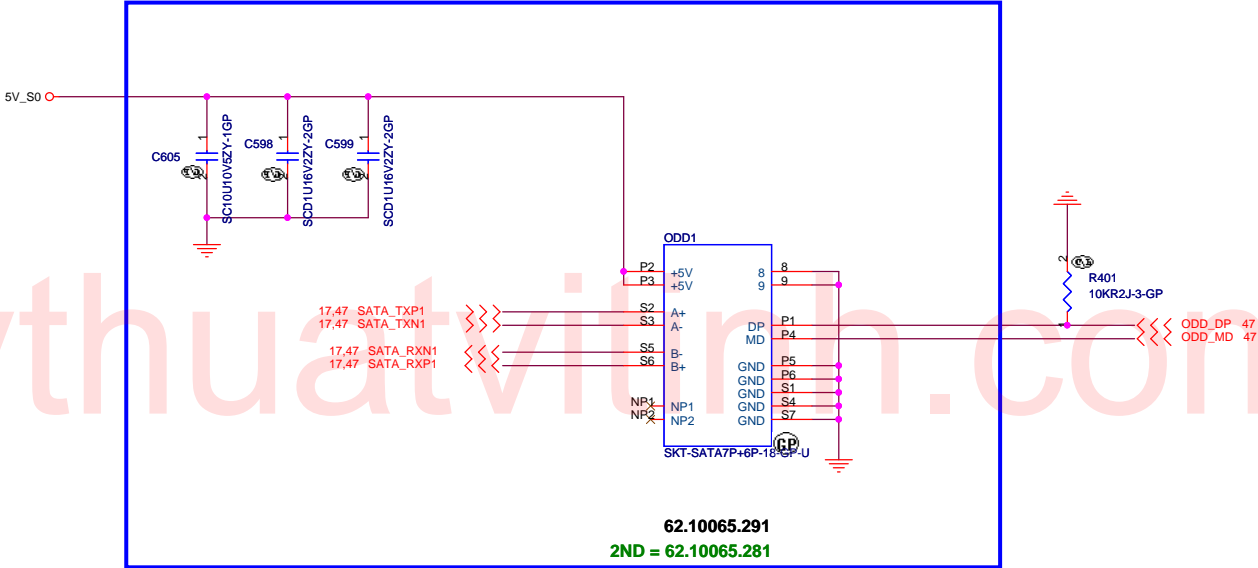
Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

SB

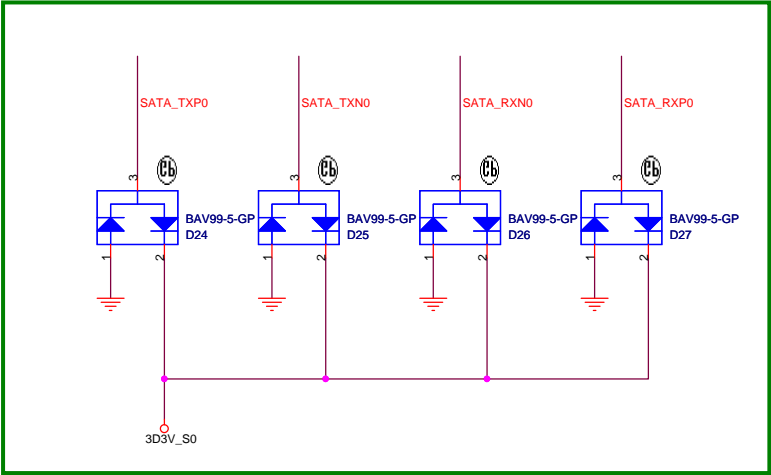
SATA HDD Connector



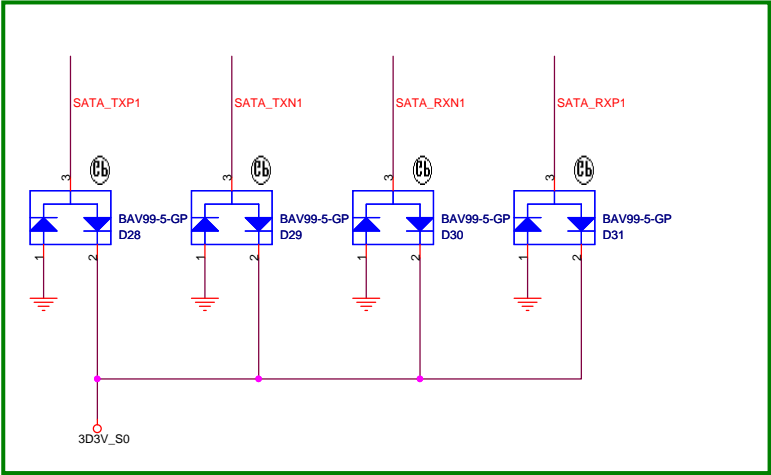
20080714 SATA ODD Connector

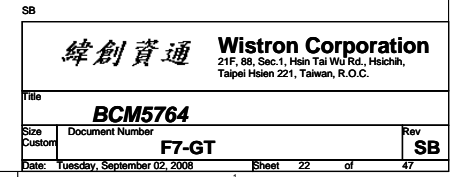


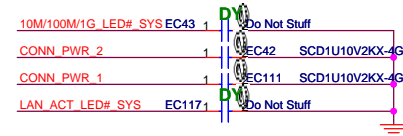
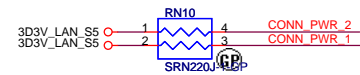
For HDD



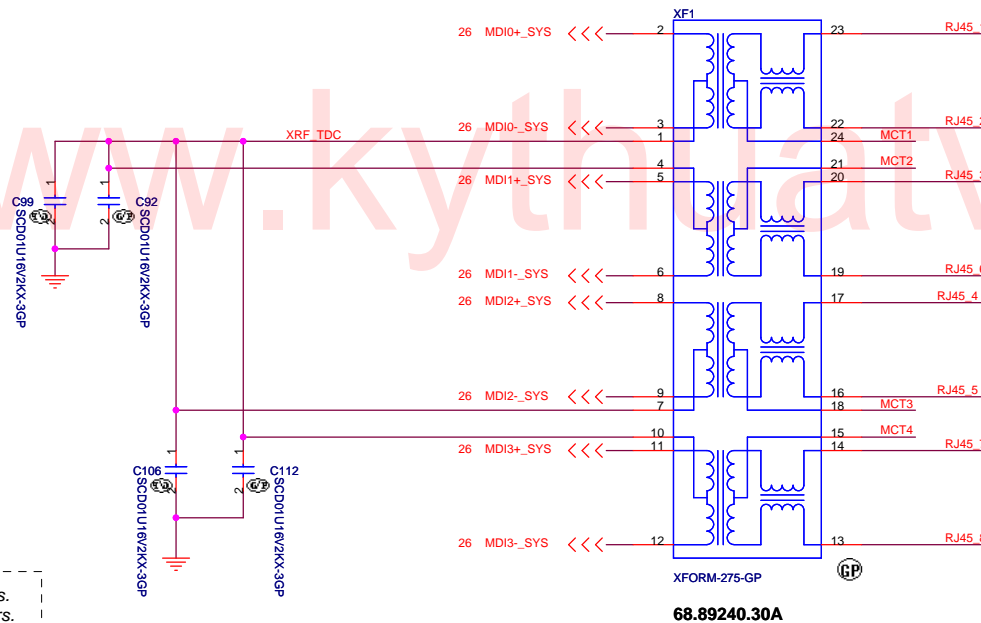
For ODD



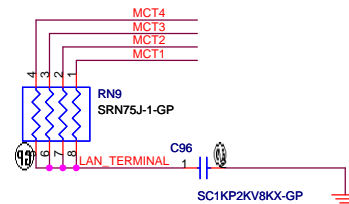




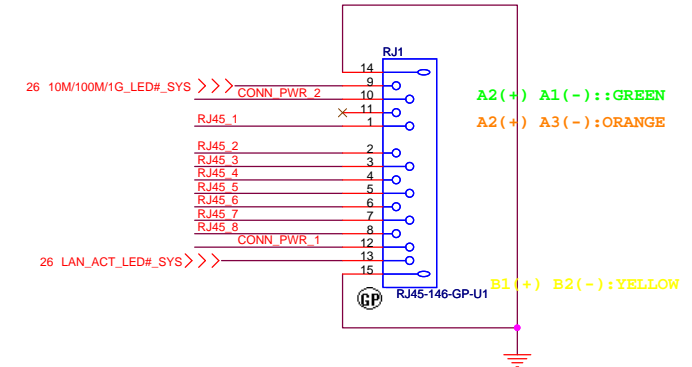
GIGA Lan Transformer



68.89240.30A



LAN Connector



22.10245.R11
2ND = 22.10245.X61

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

| 10/100 LAN Transformer | RJ45 PIN |
|------------------------|----------|
| TD+ --> TX+ | RJ45-1 |
| TD- --> TX- | RJ45-2 |
| RD+ --> RX+ | RJ45-3 |
| RD- --> RX- | RJ45-6 |

SB

緯創資通

Wistron Corporation

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Title

LAN Connector

Size A3

Document Number

F7-GT

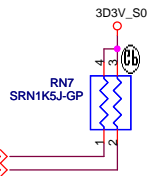
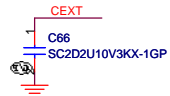
Date: Friday, August 29, 2008

Sheet 23 of 47

Rev

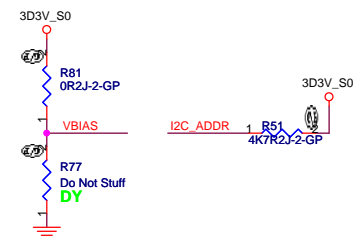
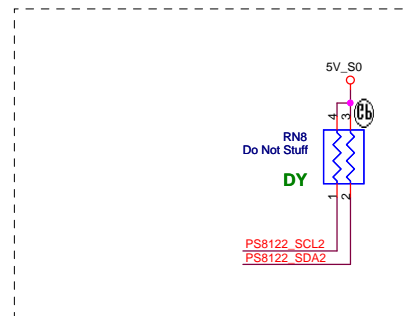
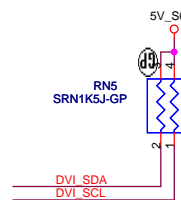
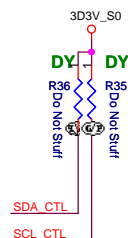
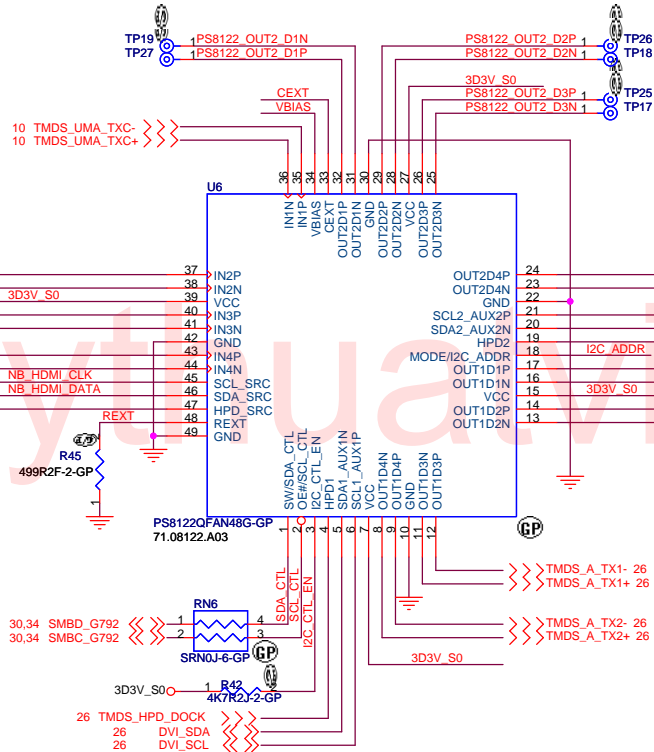
SB

11 NB_HDMI_DATA
11 NB_HDMI_CLK



10 TMDS_UMA_TX0-
10 TMDS_UMA_TX0+
10 TMDS_UMA_TX1-
10 TMDS_UMA_TX1+
10 TMDS_UMA_TX2-
10 TMDS_UMA_TX2+
11 NB_HDMI_HPD

10 TMDS_UMA_TXC-
10 TMDS_UMA_TXC+

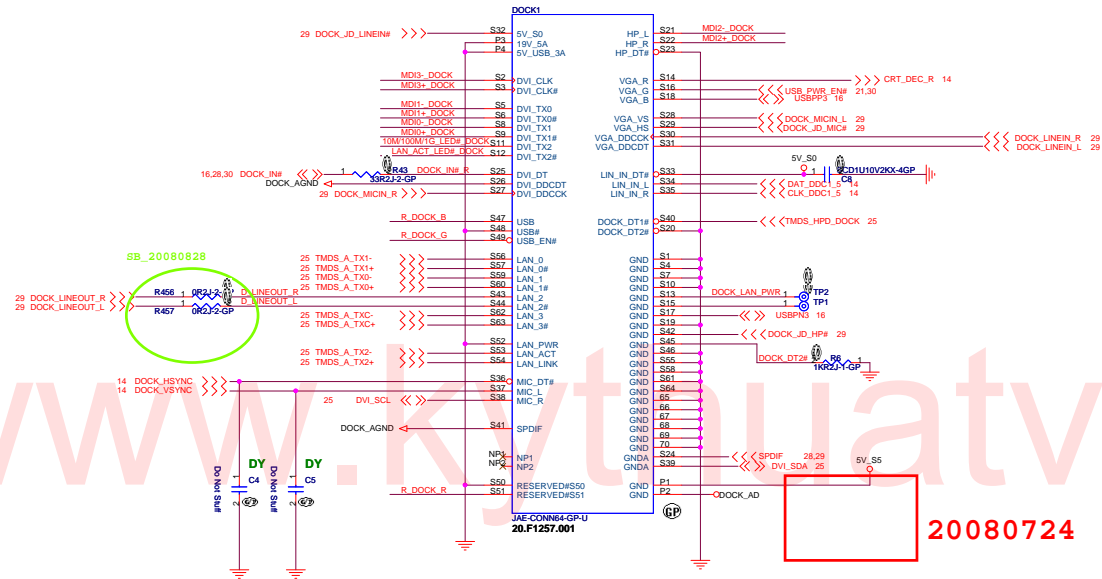


SB

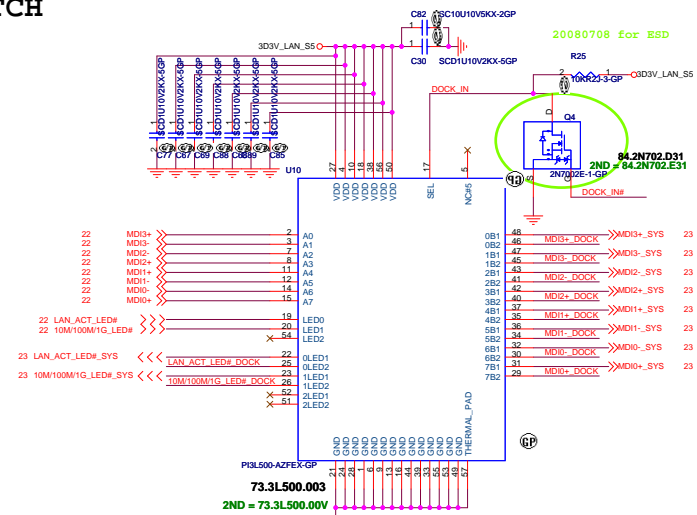
| | |
|--|----------------|
| 緯創資通 Wistron Corporation | |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title PS8122 | |
| Size Document Number | Rev SB |
| F7-GT | |
| Date: Friday, August 29, 2008 | Sheet 25 of 47 |

20080709 change to Port Replicator

DOCK

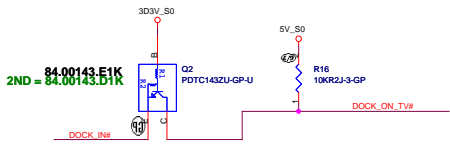


LAN SWITCH

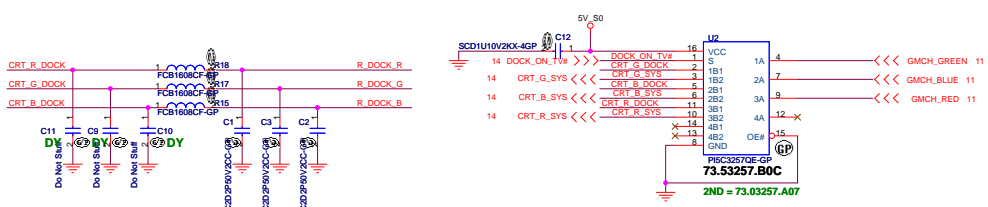


| | |
|----------|-----|
| Function | LAN |
| SYSTEM | L |
| DOCK | H |

CRT SWITCH



| Function | CRT | TV |
|----------|-----|----|
| SYSTEM | H | H |
| DOCK | L | L |

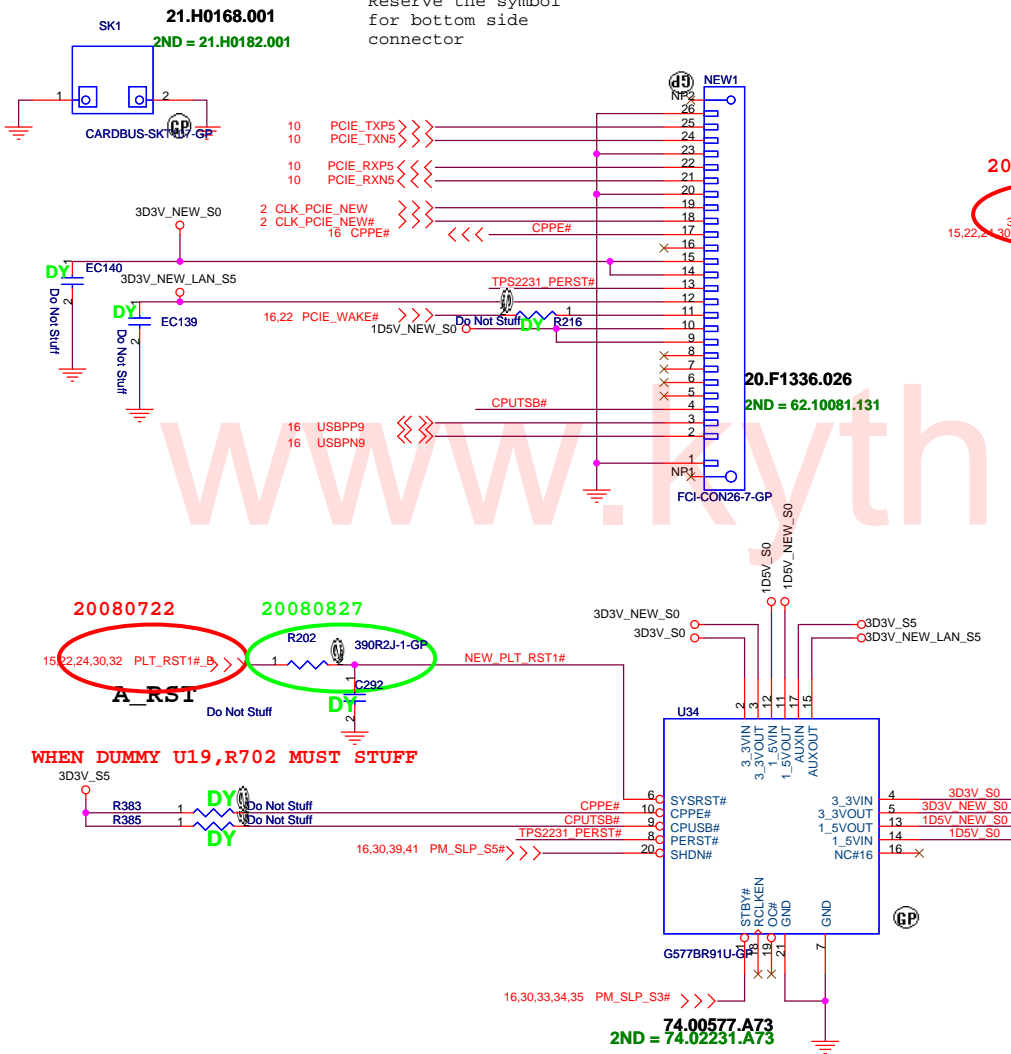


NEWCARD Connector

Mini Card Connector

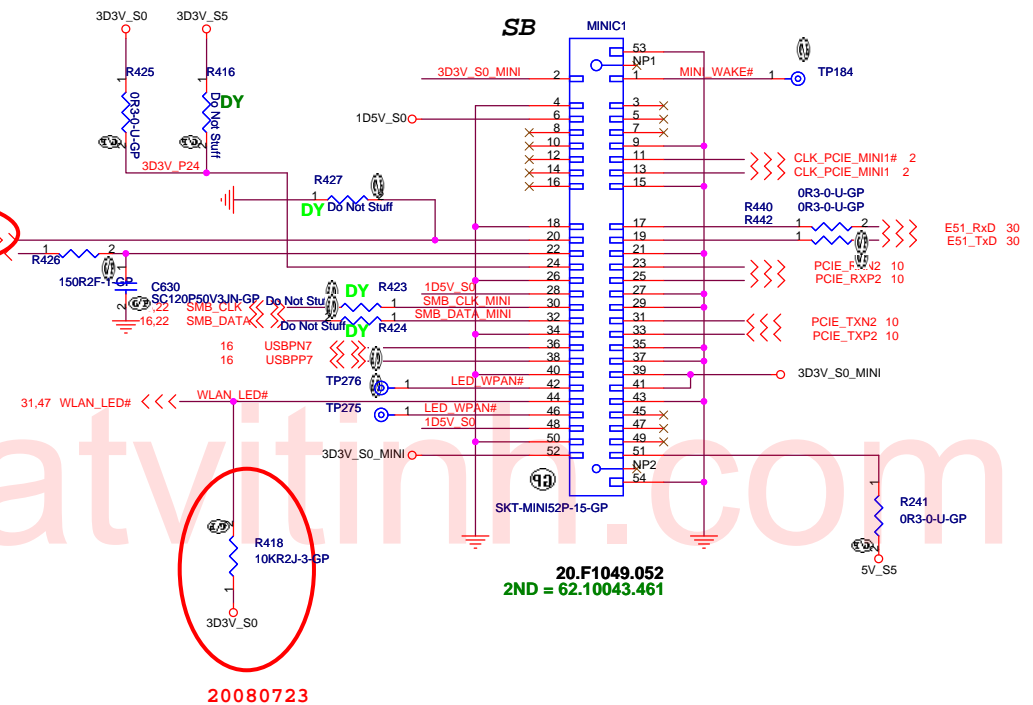
CHECK /POWER PIN

Reserve the symbol
for bottom side
connector

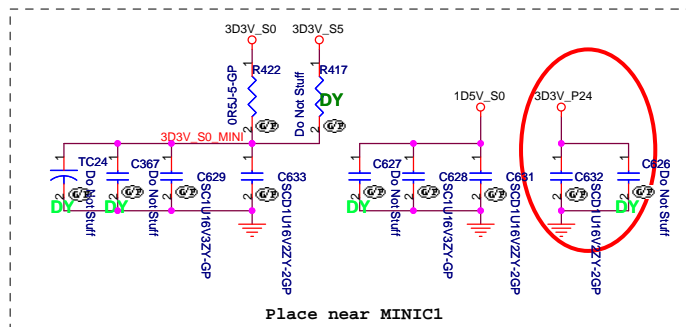
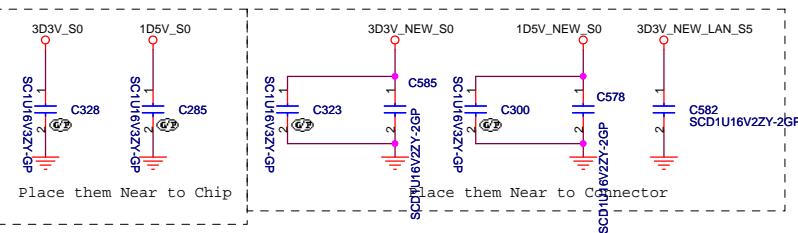


20080722
30 WIRELESS_EN
15,22,24,30,32 PLT_RST1#_B

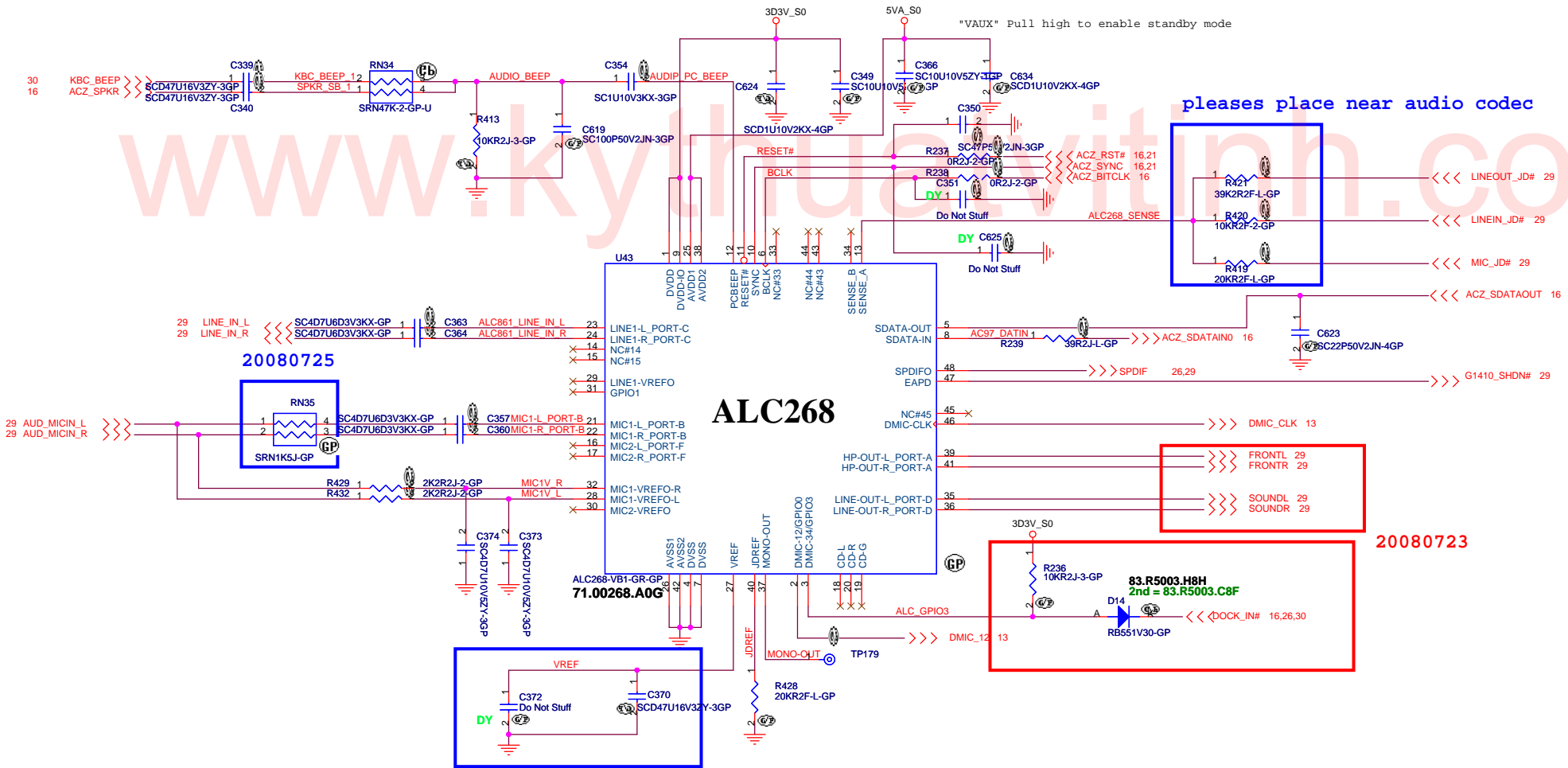
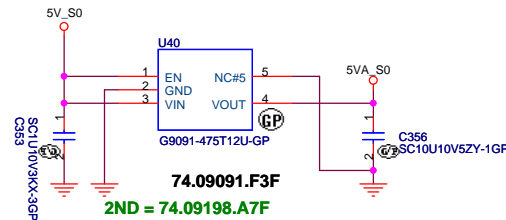
A_RST

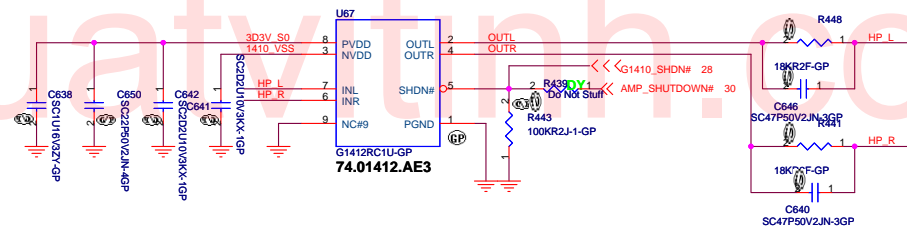
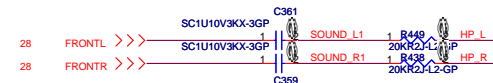
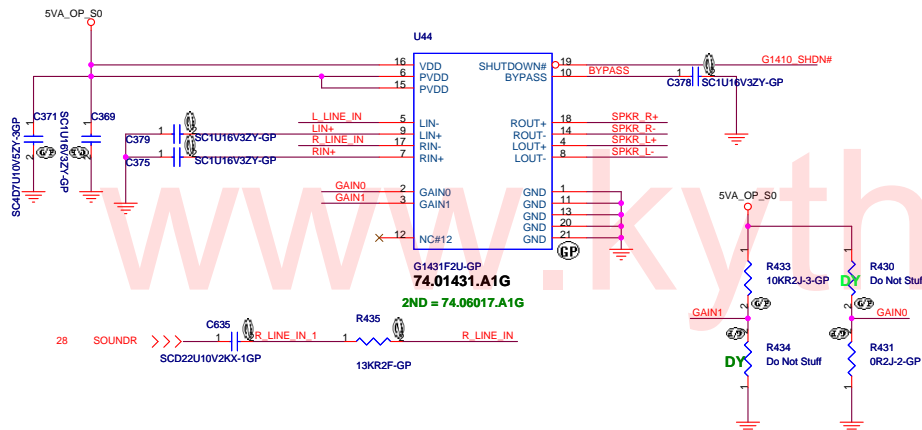
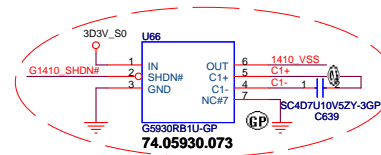
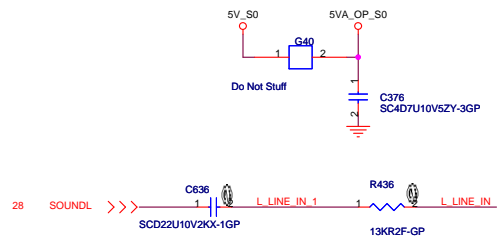


CHECK WITH COLUMBIA

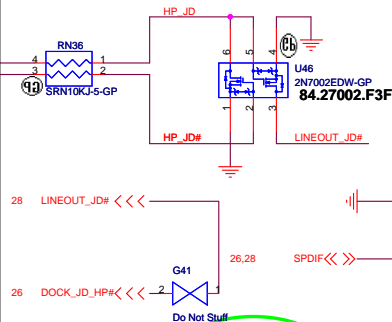
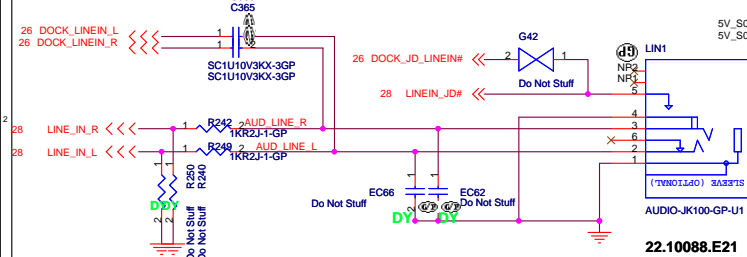


| | |
|--|------------------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| MINI CARD / NEW CARD | |
| Title F7-GT | Rev SB |
| Date: Tuesday, September 02, 2008 | Sheet 27 of 47 |

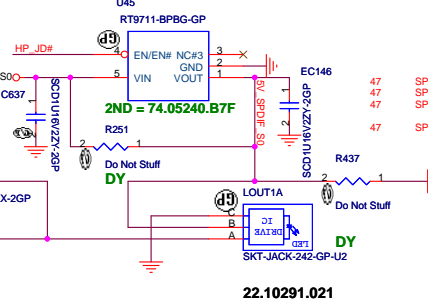




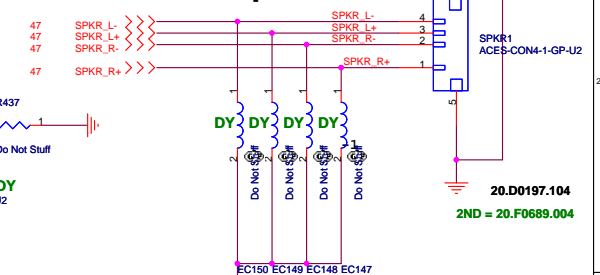
LINE IN



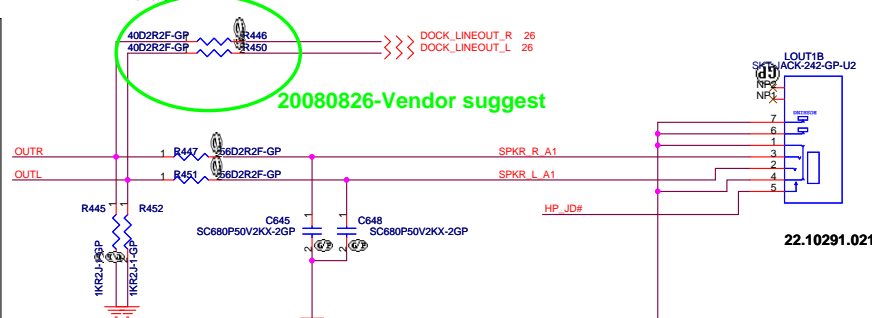
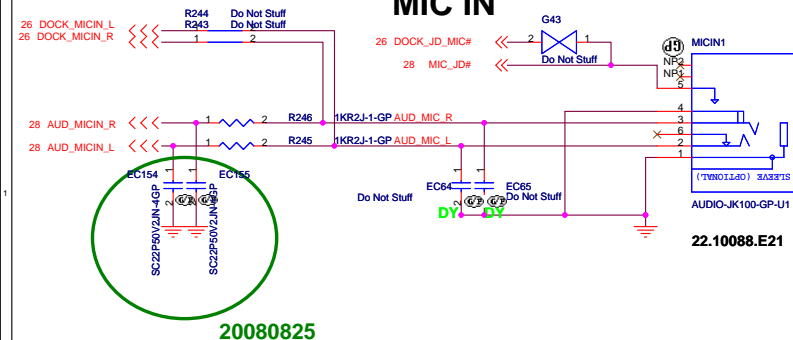
74.09711.07F



Internal Speaker

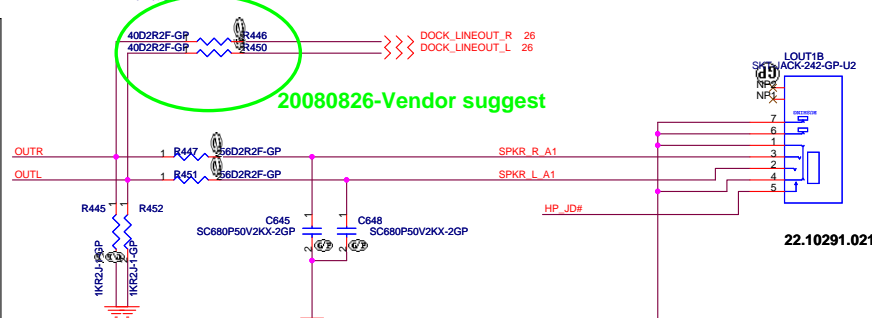


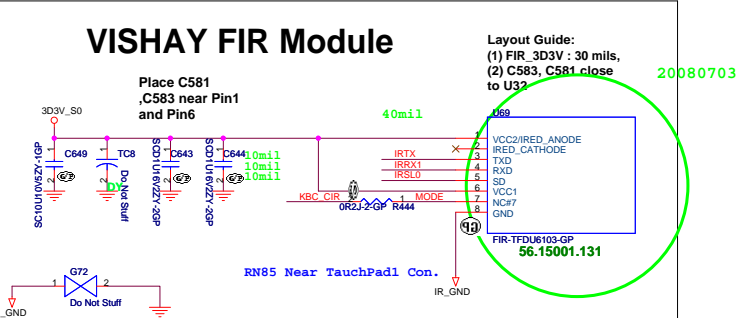
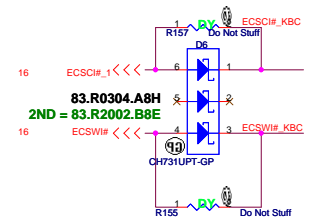
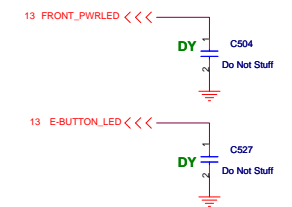
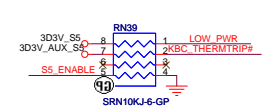
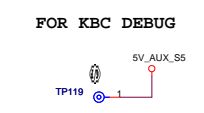
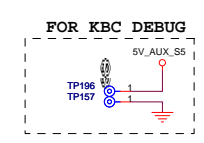
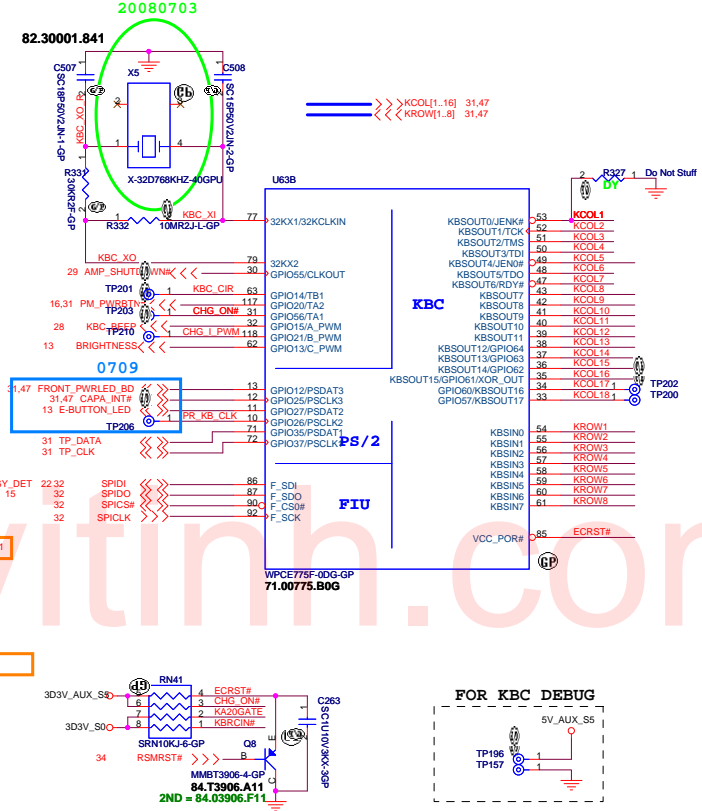
MIC IN



20080826-Vendor suggest

LINE OUT

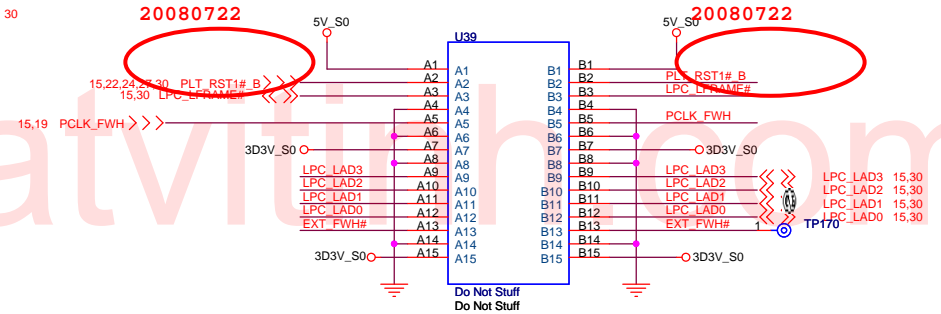


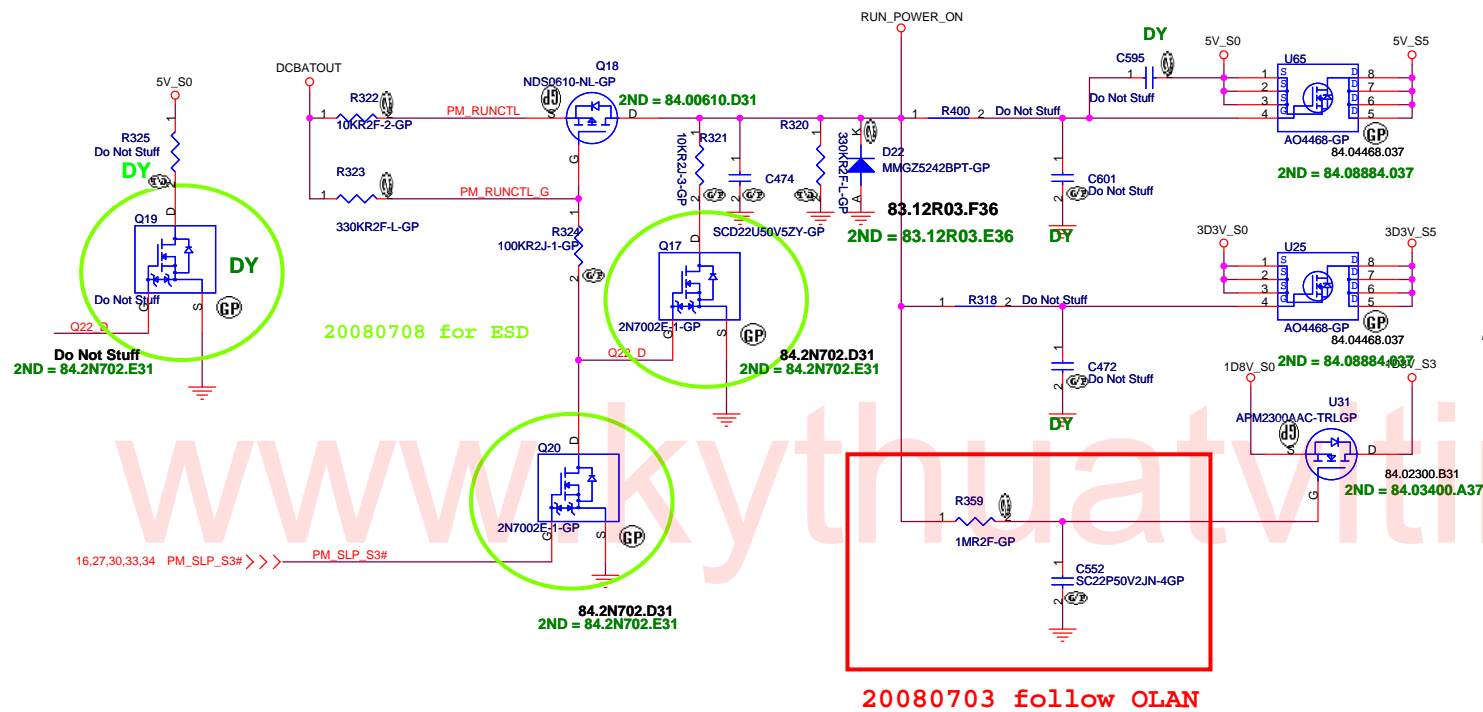


16M Bits



20080722

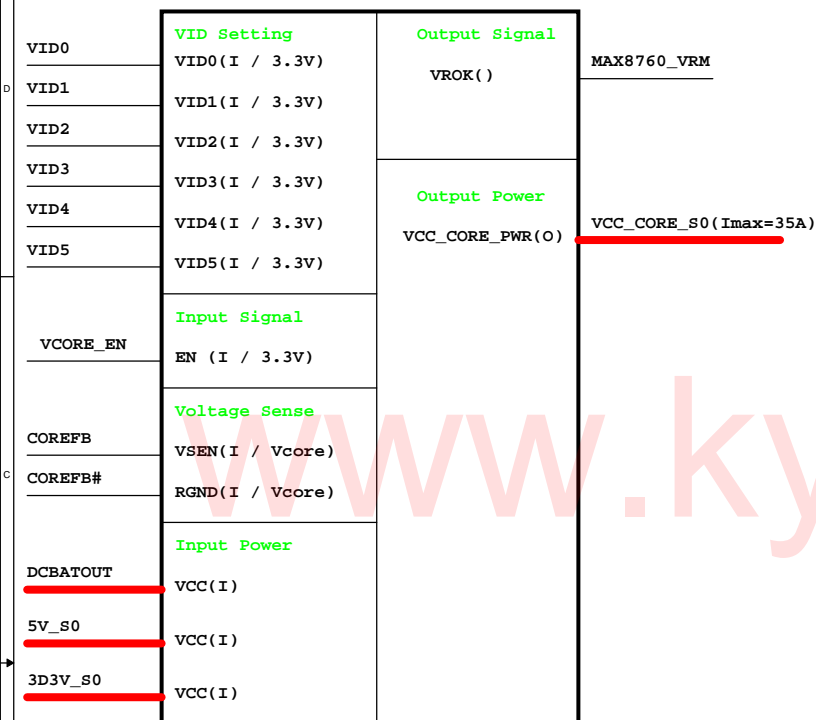




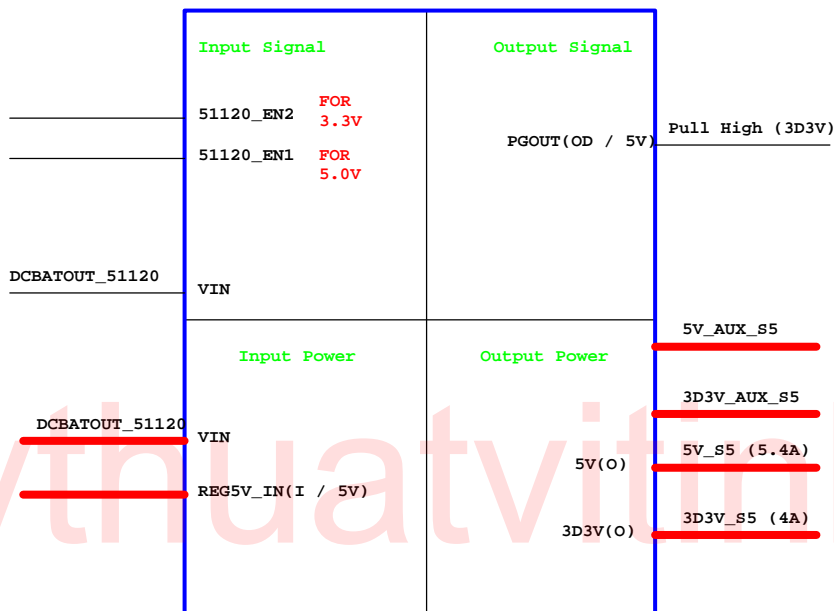
SB

| | | | |
|----------------------------------|-----------------|---|-------|
| 緯創資通 | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| PWR CTL LOGIC / PWR PLANE | | | |
| Size | Document Number | Rev | |
| A3 | | SB | |
| F7-GT | | | |
| Date: Friday, August 29, 2008 | | Sheet 35 | of 47 |

CPU_CORE
ISL6264CRZ



TI TPS51120
3D3V/5V

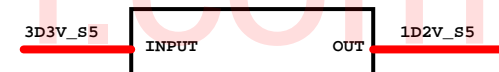


2D5V_S0



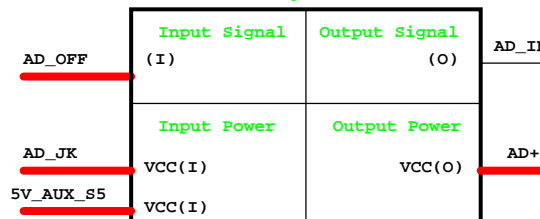
APL5913

1D8V_S5

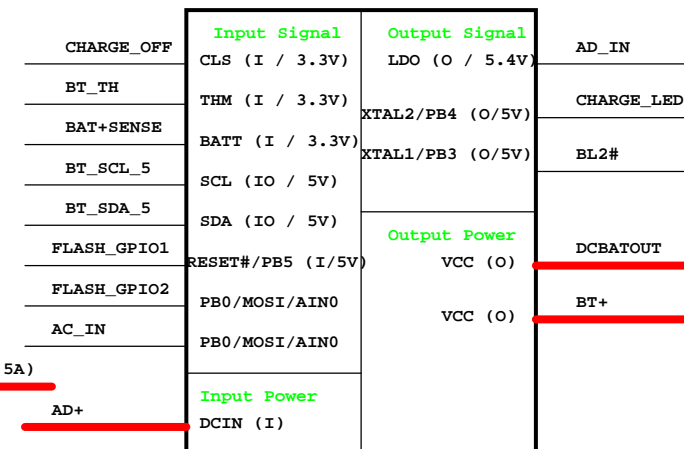


APL5332KAC-TRLGP

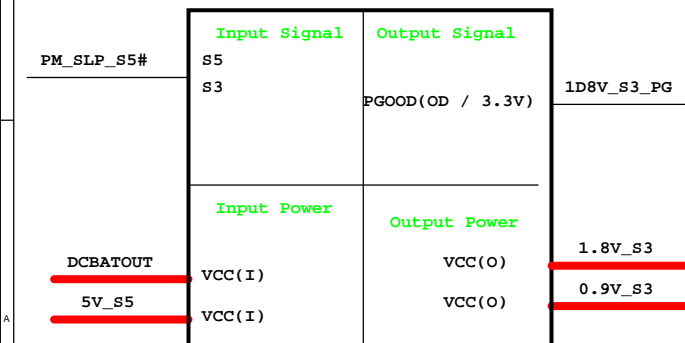
Adapter



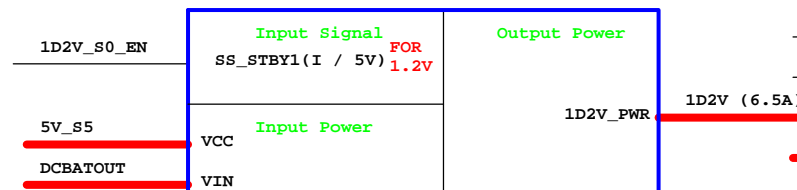
Charger_ISL6255



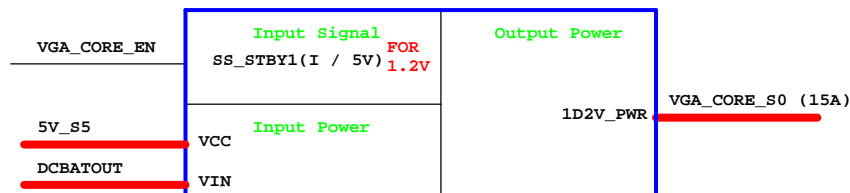
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V

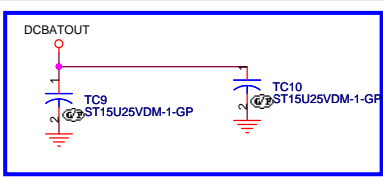


ISL6268_VGA_CORE



SB

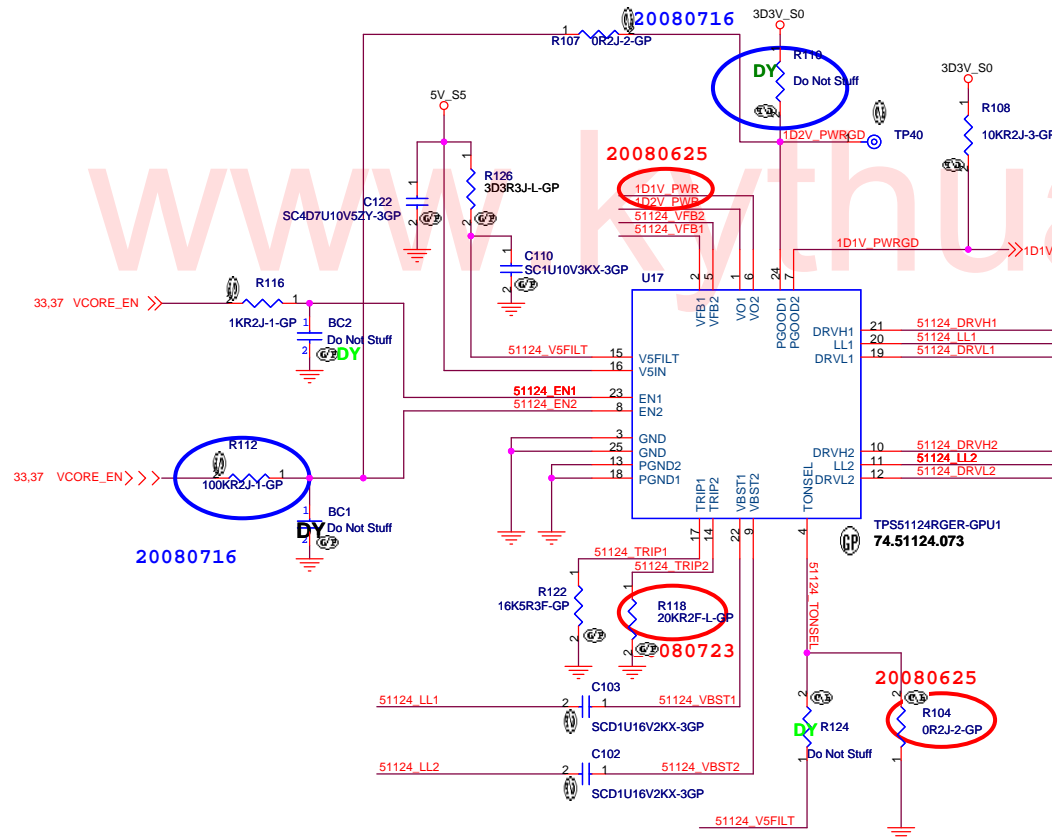
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| 緯創資通 Wistron Corporation | |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | |
| Power Block Diagram | |
| Size A3 | Document Number |
| F7-GT | |
| Date: Tuesday, August 19, 2008 | Sheet 36 of 47 |
| Rev SB | |



SB_20080827

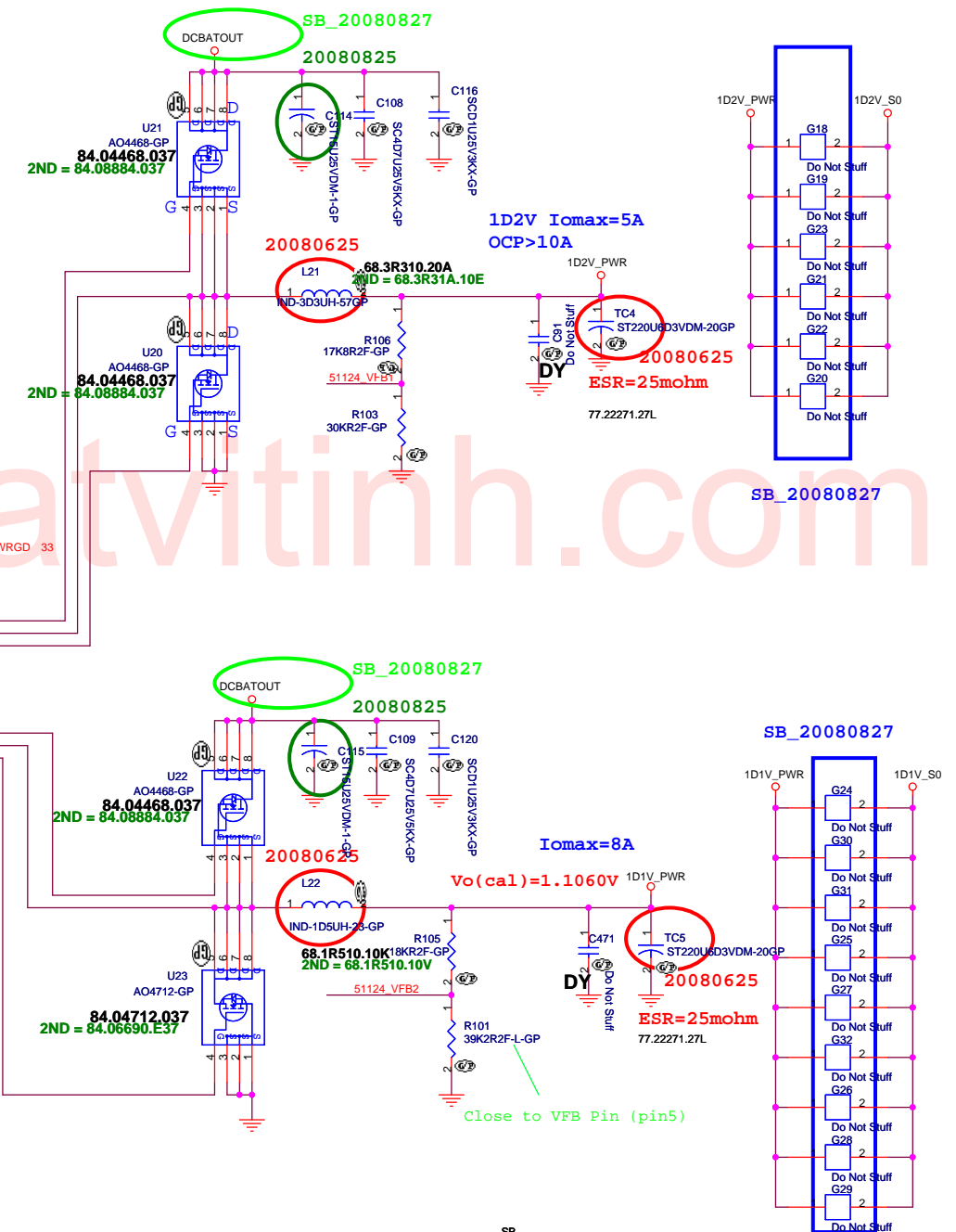
$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$$

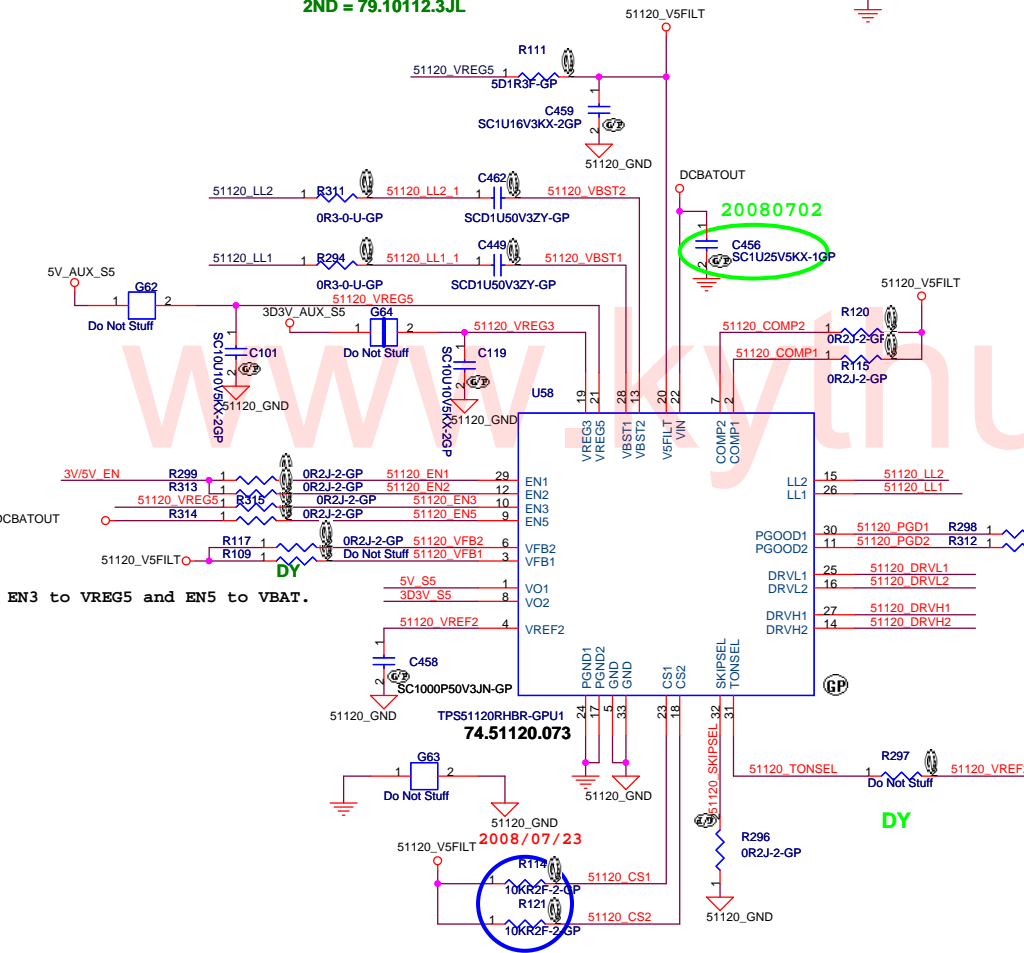
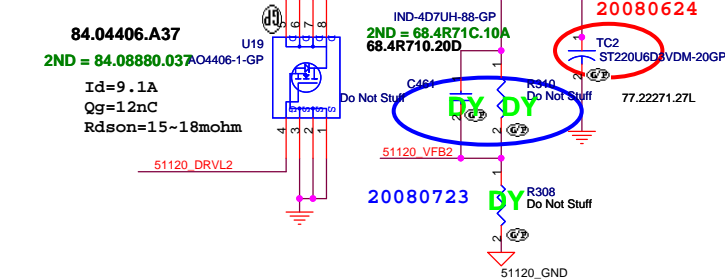
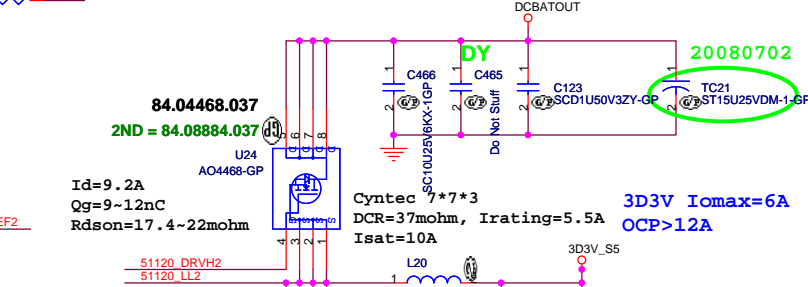
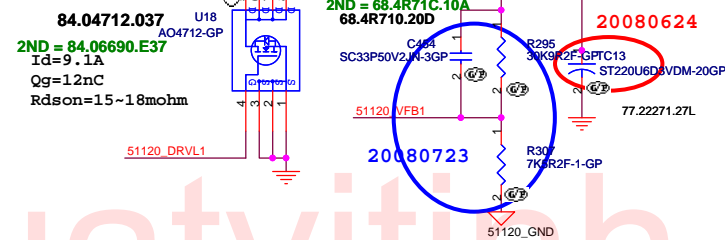
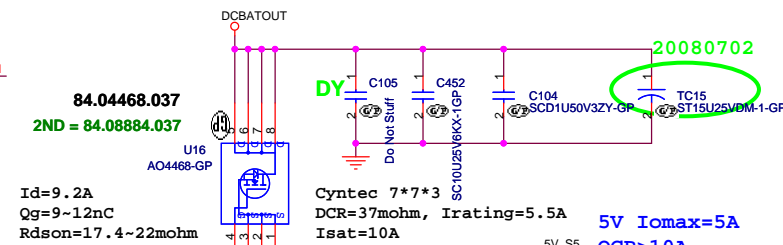


| | GND | OPEN | V5FILT |
|--------|----------------------|----------------------|----------------------|
| TONSEL | 240k/CH1 300k/CH2 | 300k/CH1 360k/CH2 | 360k/CH1 420k/CH2 |

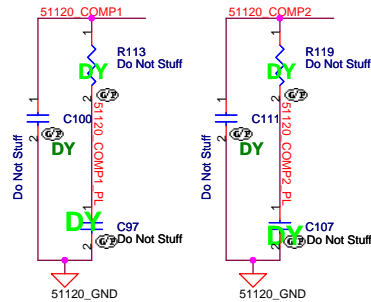
$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode



SB



| | GND | VREF2 | FLOAT | V5FILT |
|---------|----------------------|-----------------------|----------------------|----------------------|
| SKIPSEL | AUTOSKIP | AUTOSKIP / FAULTS OFF | PWM | PWM |
| COMP | N/A | N/A | CURRENT MODE | D-Cap MODE |
| TONSEL | 380k/CH1 590k/CH2 | 290k/CH1 440k/CH2 | 220k/CH1 330k/CH2 | 180k/CH1 280k/CH2 |
| VFB1 | N/A | not use | ADJ. | 5V Fixed Output |
| VFB2 | N/A | not use | ADJ. | 3.3V Fixed Output |
| EN1,EN2 | switcher OFF | not use | Swither ON | Switcher ON |
| EN3,EN5 | LDO OFF | not use | LDO ON | VREG3 on |



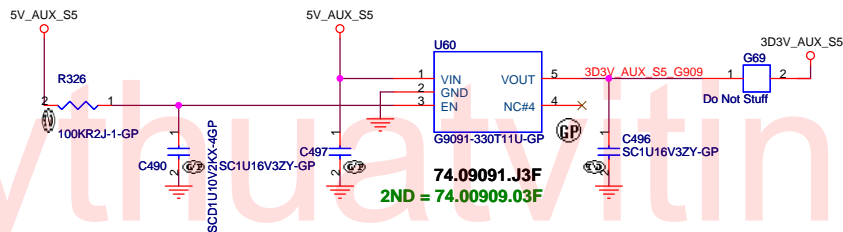
For TP51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

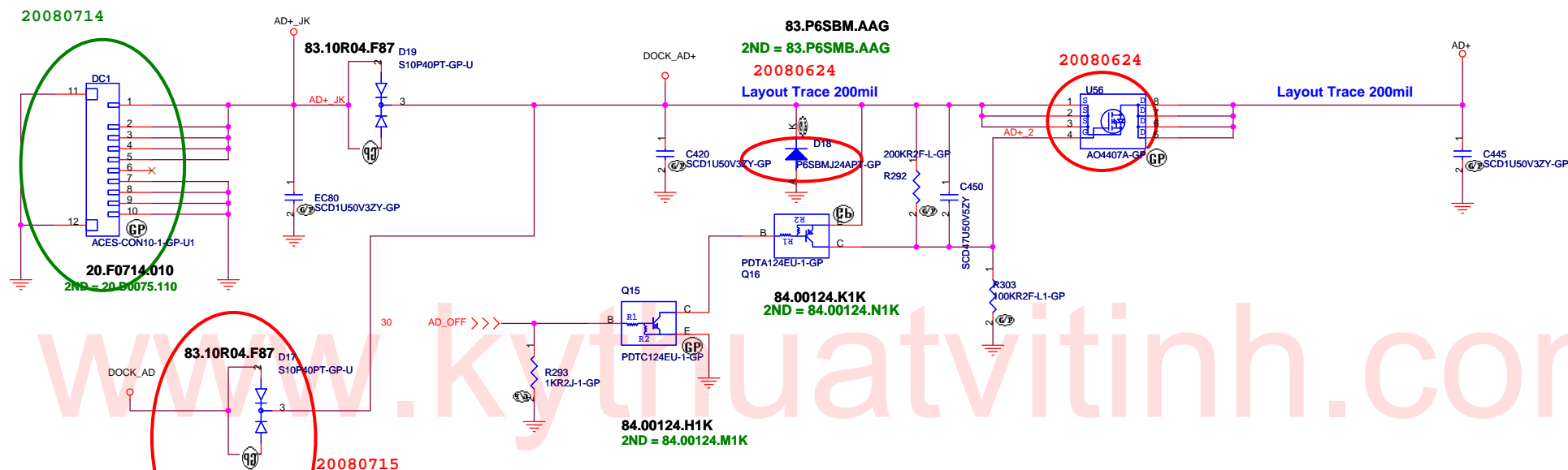
Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

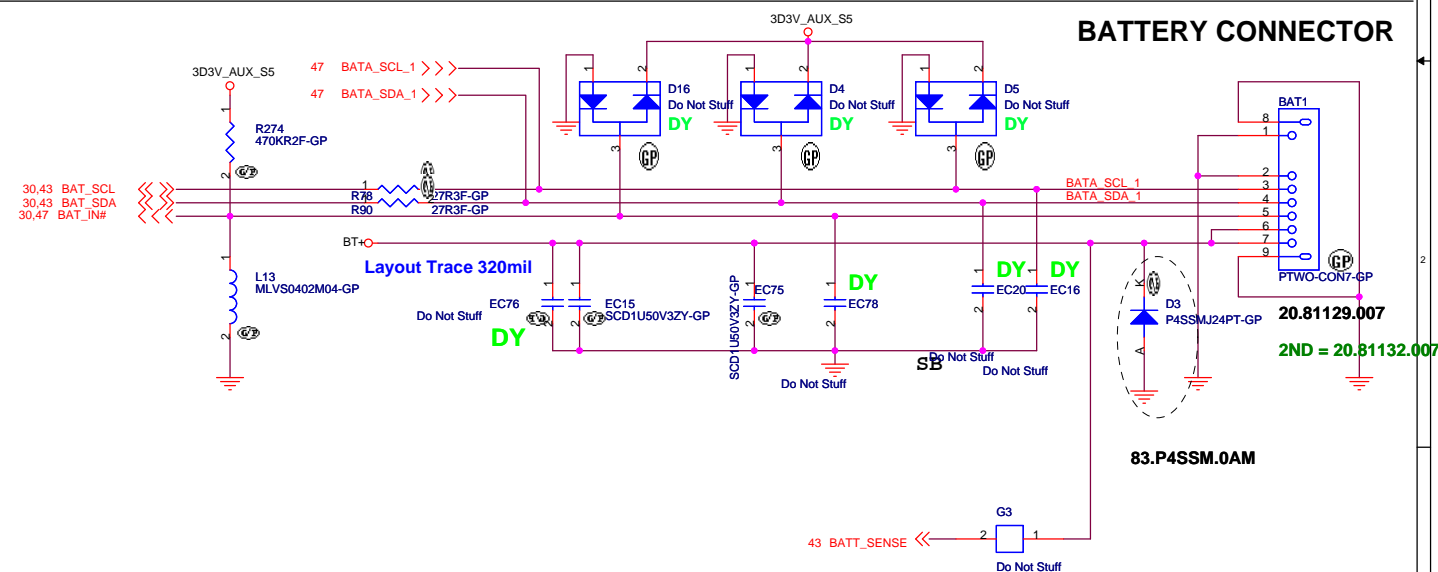
Aux Power 3D3V_AUX_S5



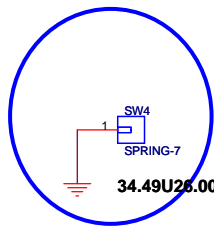
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

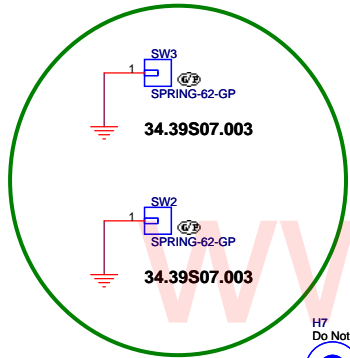


SB_20080827



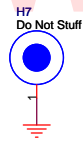
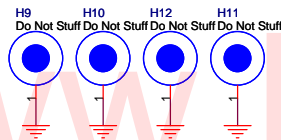
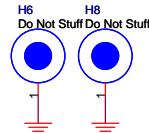
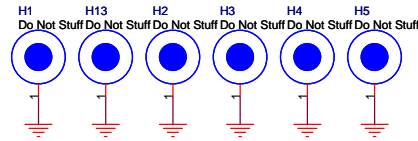
34.49U26.001

20080725



34.39S07.003

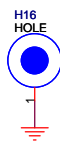
34.39S07.003



34.41Q08.011

34.41Q08.011

34.41Q08.011

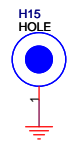


34.4P910.001



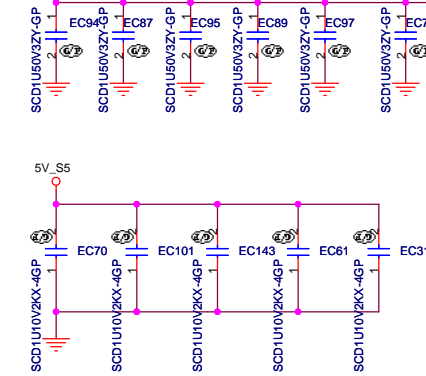
34.4G502.011

34.4G502.011

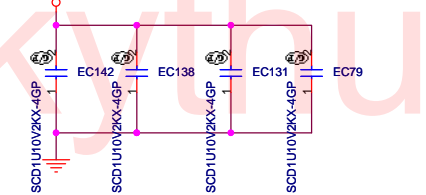


34.41Q08.011

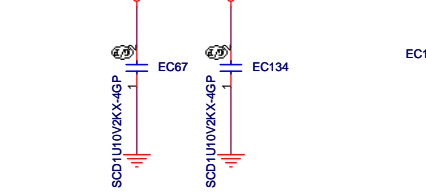
DCBATOUT



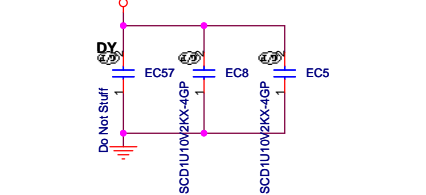
5V_S5



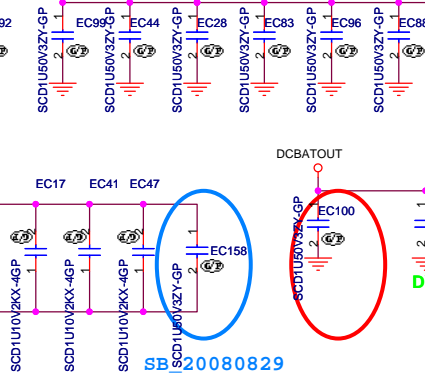
3D3V_S5



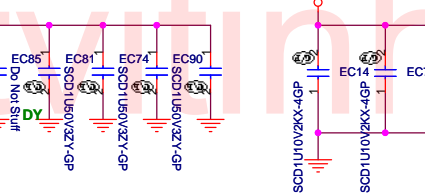
3D3V_S0



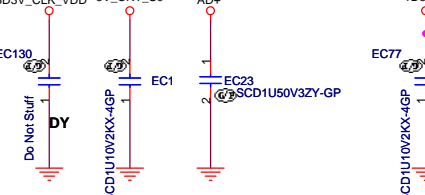
DCBATOUT



5V_S0



DOCK_AD+



3D3V_LAN_S5



3D3V_CLK_VDD



5V_CRT_S0

AD+

1D8V_S3

DOCK_AD

20080702

SB_20080828

SB_20080829


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